



SPP9972

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP9972 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology. The SPP9972 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

FEATURES

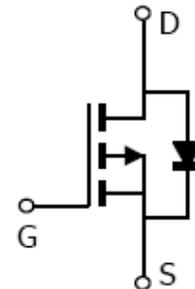
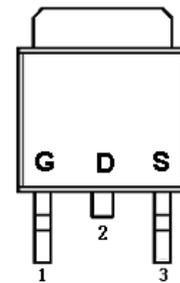
- ◆ $-60V/-18A, R_{DS(ON)}=25m\Omega @ V_{GS}=-10V$
- ◆ $-60V/-12A, R_{DS(ON)}=33m\Omega @ V_{GS}=-4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-252-2L package design

APPLICATIONS

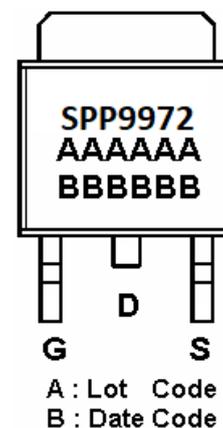
- Power Management in Note book
- Powered System
- DC/DC Converter
- Load Switch

PIN CONFIGURATION

TO-252-2L



PART MARKING





SPP9972

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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP9972T252RGB	TO-252-2L	SPP9972

※ SPP9972T252RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	-60	V	
Gate –Source Voltage	V _{GSS}	±20	V	
Continuous Drain Current(T _J =150°C)	I _D	T _A =25°C	-35	A
		T _A =100°C	-27	
Pulsed Drain Current	I _{DM}	-70	A	
Single Pulse Avalanche Energy	E _{AS}	162	mJ	
Power Dissipation	P _D	52	W	
Operating Junction Temperature	T _J	-55/150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Case	R _{θJC}	2.4	°C/W	



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ELECTRICAL CHARACTERISTICS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1		-2.5	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-48V, V_{GS}=0V$			-1	uA
		$V_{DS}=-48V, V_{GS}=0V$ $T_J=55^\circ C$			-5	
On-State Drain Current	$I_{D(on)}$	$V_{DS}=0V, V_{GS}=0V$			-35	A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-18A$		0.02	0.025	Ω
		$V_{GS}=-4.5V, I_D=-12A$		0.026	0.033	
Forward Transconductance	g_{fs}	$V_{DS}=-10V, I_D=-18A$		23		S
Diode Forward Voltage	V_{SD}	$I_S=-1A, V_{GS}=0V$			-1	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-20V, V_{GS}=-4.5V$ $I_D=-12A$		25		nC
Gate-Source Charge	Q_{gs}			6.7		
Gate-Drain Charge	Q_{gd}			5.5		
Input Capacitance	C_{iss}	$V_{DS}=-15V, V_{GS}=0V$ $f=1MHz$		3635		pF
Output Capacitance	C_{oss}			225		
Reverse Transfer Capacitance	C_{rss}			140		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-15V, I_D=-1A,$ $V_{GEN}=-10V, R_G=3.3\Omega$		38		nS
	t_r			24		
Turn-Off Time	$t_{d(off)}$			100		
	t_f			7		



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TYPICAL CHARACTERISTICS

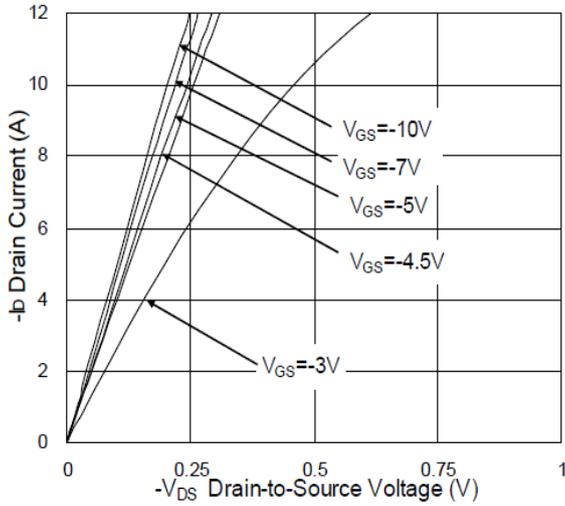


Fig 1. Output Characteristic

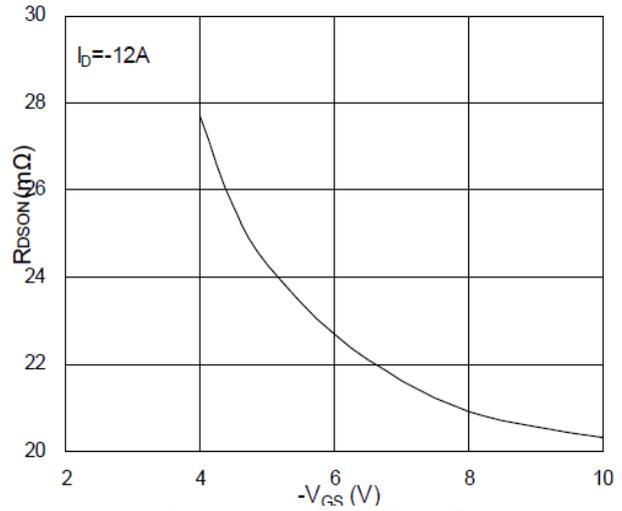


Fig 2. On Resistance vs Gate Source Voltage

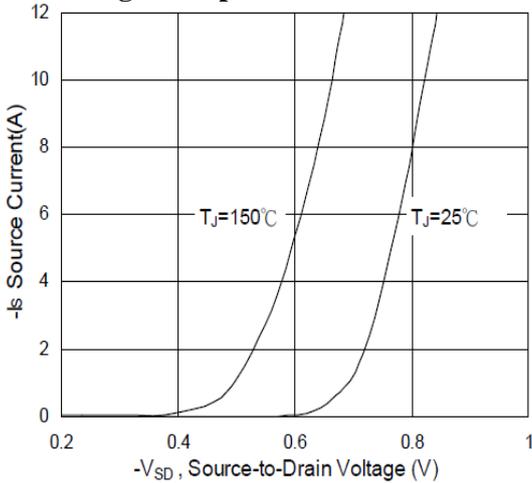


Fig 3. Source-Drain Diode Forward Voltage

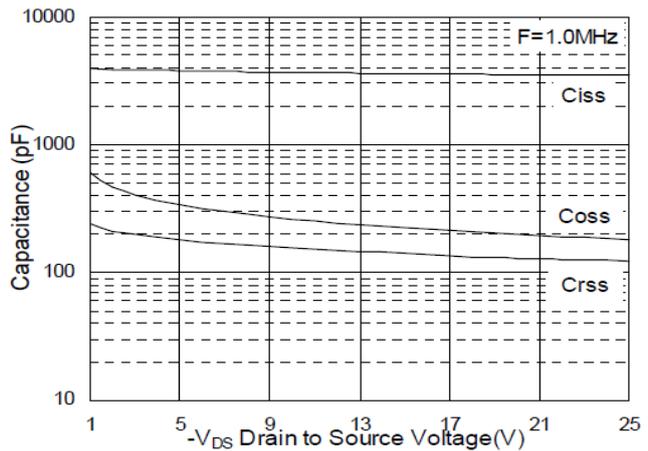


Fig 4. Capacitance

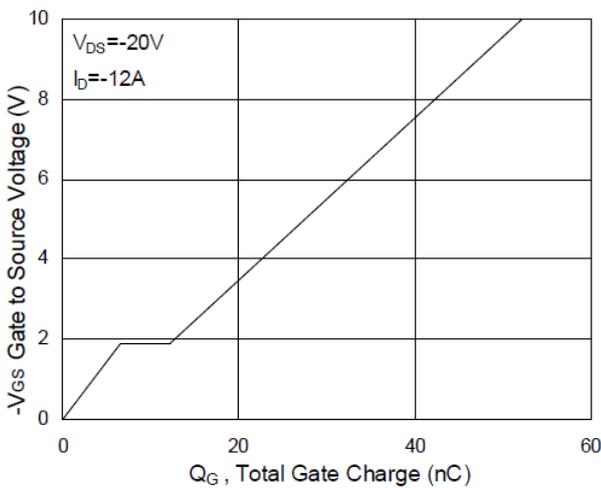


Fig 5. Gate Charge

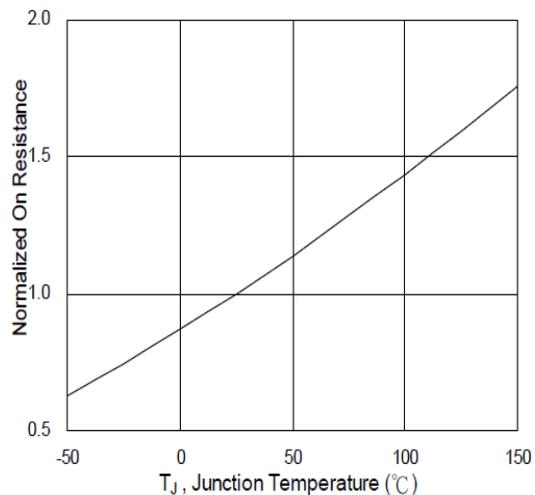


Fig 6. On Resistance vs Junction Temperature



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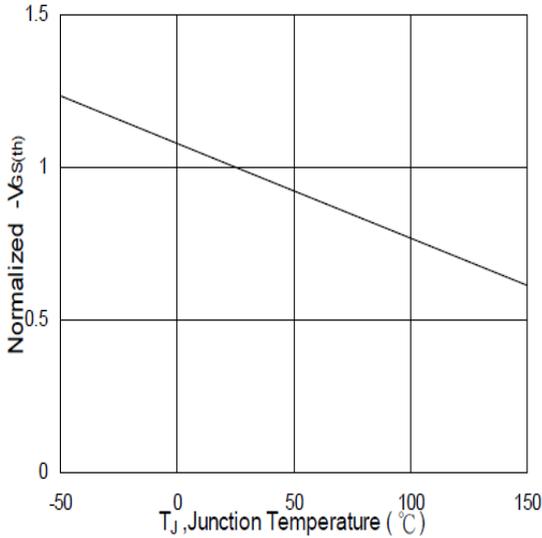


Fig. 7 Threshold Voltage vs Temperature

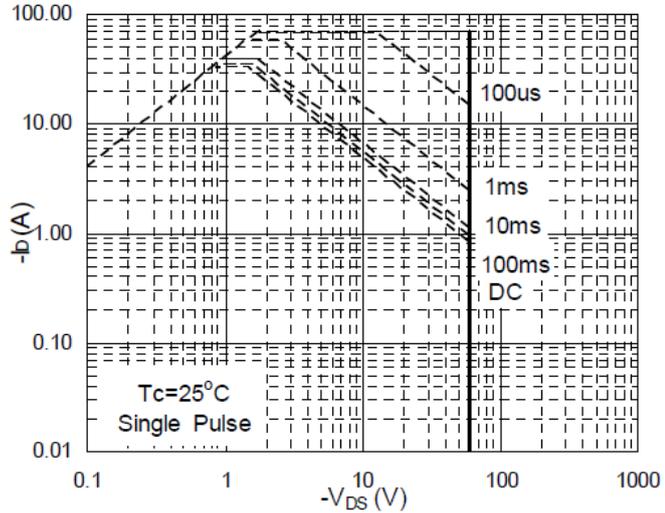


Fig. 8 Safe Operating Rnpage

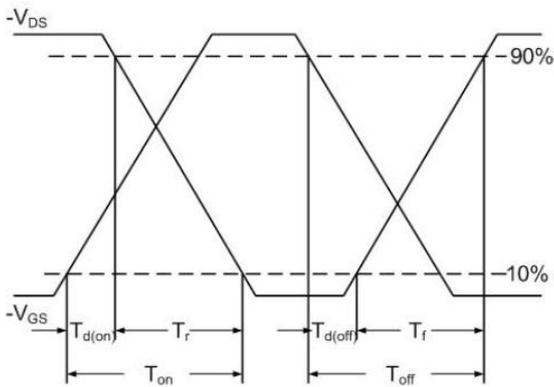


Fig 9. Switching Time Waveform

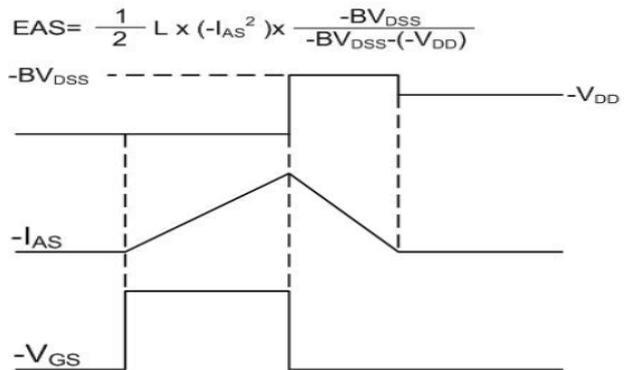


Fig. 10 Unclamped Inductive Waveform

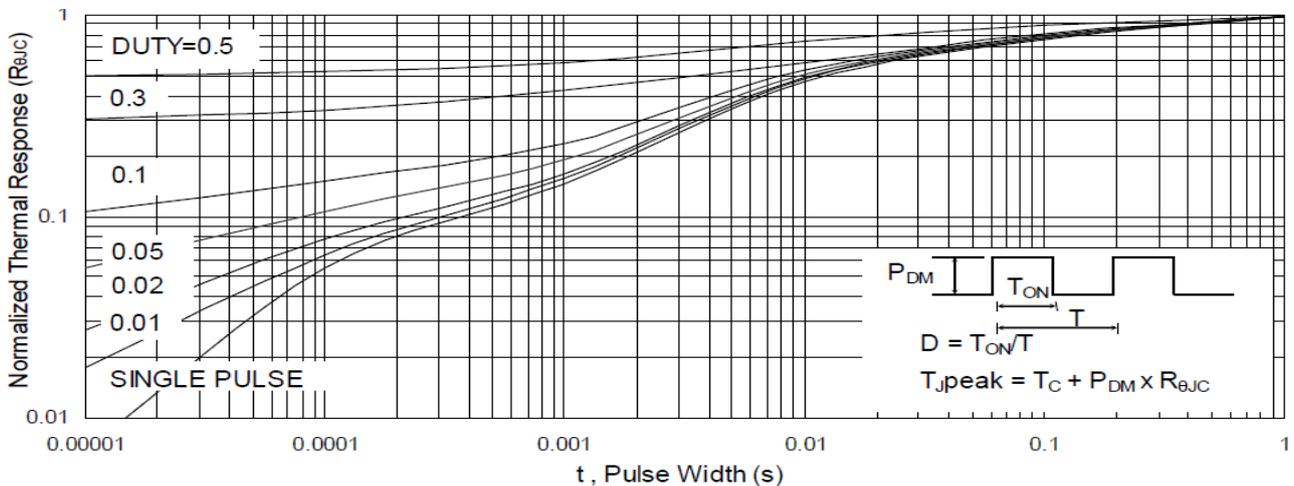


Fig 11. Maximum Transient Thermal Impedance



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SYNC Power Corporation

7F-2, No.3-1, Park Street

NanKang District (NKSP), Taipei, Taiwan 115

Phone: 886-2-2655-8178

Fax: 886-2-2655-8468

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