SPP8527
Dual P-Channel Enhancement Mode

DESCRIPTION

The SPP8527 is the Dual P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

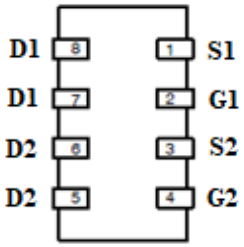
APPLICATIONS

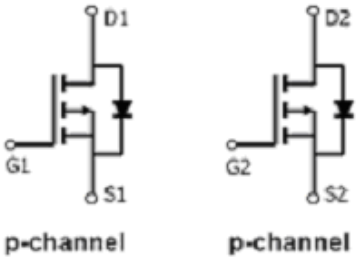
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

FEATURES

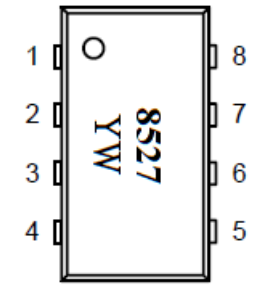
- -20V/-3.3A,$R_{DS(ON)}$=70mΩ@V_{GS}=-4.5V
- -20V/-2.8A,$R_{DS(ON)}$=85mΩ@V_{GS}=-2.5V
- -20V/-2.3A,$R_{DS(ON)}$=130mΩ@V_{GS}=-1.8V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- PPAK3x2-8L package design

PIN CONFIGURATION (PPAK3x2-8L)





PART MARKING



Y : Year Code
W : Week Code

SPP8527
Dual P-Channel Enhancement Mode

PIN DESCRIPTION

Pin	Symbol	Description
1	S1	Source 1
2	G1	Gate 1
3	S2	Source 2
4	G2	Gate 2
5	D2	Drain 2
6	D2	Drain 2
7	D1	Drain 1
8	D1	Drain 1

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP8527DN8RGB	PPAK3x2-8L	8527

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)
※ SPP8527DN8RGB : Tape Reel ; Pb – Free; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

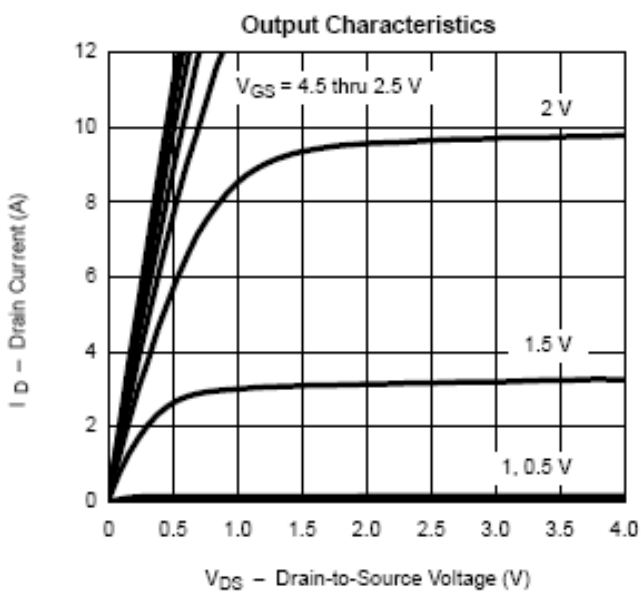
Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-20	V
Gate –Source Voltage		V_{GSS}	±12	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	-3.5	A
	T_A=70℃		-2.8	
Pulsed Drain Current		I_{DM}	-10	A
Continuous Source Current(Diode Conduction)		I_S	-1.6	A
Power Dissipation	T_A=25℃	P_D	1.25	W
	T_A=70℃		0.8	
Operating Junction Temperature		T_J	150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	120	℃/W

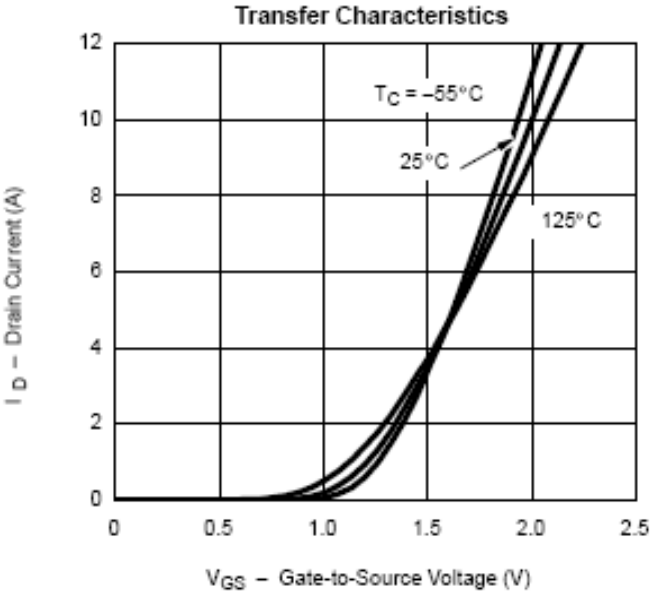
ELECTRICAL CHARACTERISTICS

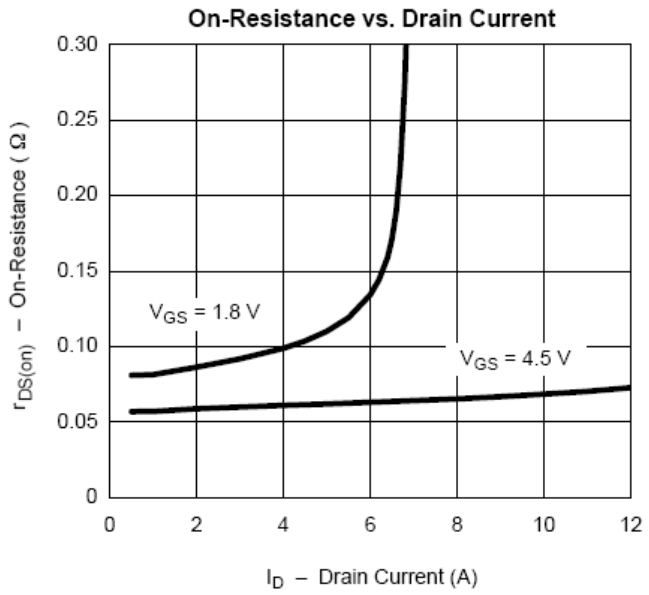
(T_A=25℃ Unless otherwise noted)

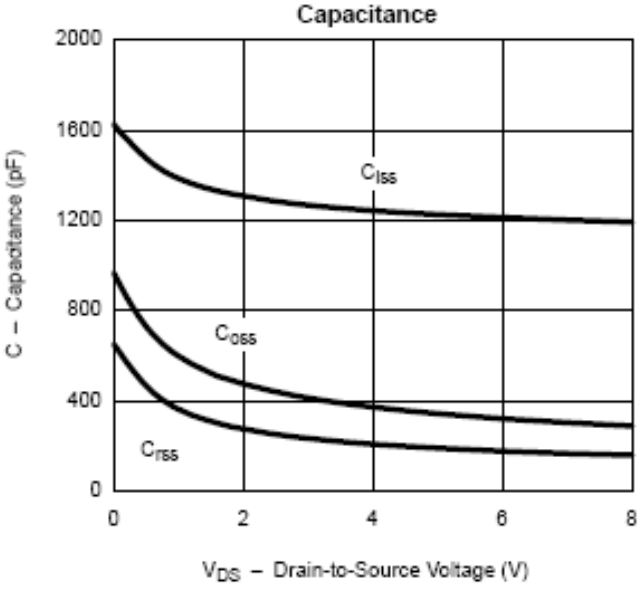
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250uA	-0.45		-0.90	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±10V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-16V,V_{GS}=0V			-1	uA
		V_{DS}=-16V,V_{GS}=0V T_J=55℃			-10	
On-State Drain Current	$I_{D(on)}$	V_{DS}≦-5V,V_{GS}=-4.5V	-4			A
		V_{DS}≦-5V,V_{GS}=-2.5V	-2			
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-4.5V,I_D=-3.3A		60	70	mΩ
		V_{GS}=-2.5V,I_D=-2.8A		72	85	
		V_{GS}=-1.8V,I_D=-2.3A		115	130	
Forward Transconductance	gfs	V_{DS}=-5V,I_D=-3.5A		8.5		S
Diode Forward Voltage	V_{SD}	I_S=-1.5A,V_{GS}=0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-6V,V_{GS}=-4.5V I_D=-2.8A		4.8	8	nC
Gate-Source Charge	Q_{gs}			1.0		
Gate-Drain Charge	Q_{gd}			1.0		
Input Capacitance	C_{iss}	V_{DS}=-6V,V_{GS}=0V f=1MHz		485		pF
Output Capacitance	C_{oss}			85		
Reverse Transfer Capacitance	C_{rss}			40		
Turn-On Time	$t_{d(on)}$	V_{DD}=-6V,R_L=6Ω I_D=-1.0A,V_{GEN}=-4.5V R_G=6Ω		10	16	nS
	t_r			13	23	
Turn-Off Time	$t_{d(off)}$			18	25	
	t_f			15	20	

TYPICAL CHARACTERISTICS



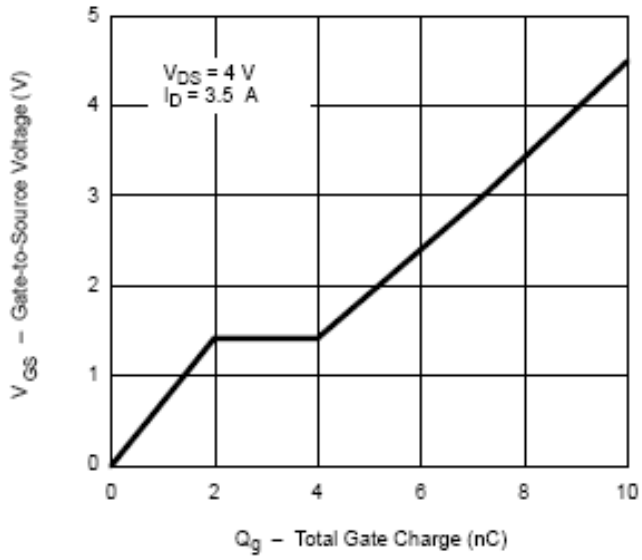




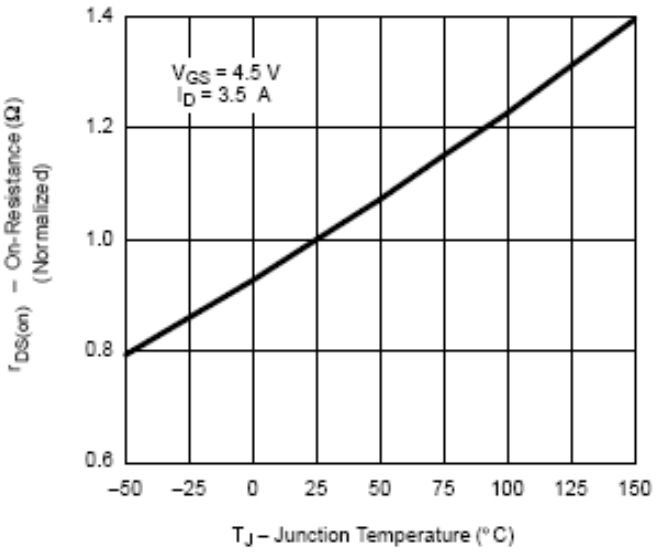


TYPICAL CHARACTERISTICS

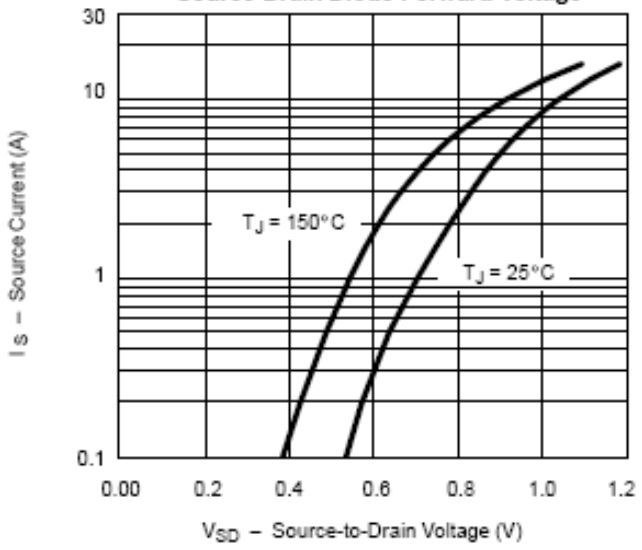
Gate Charge



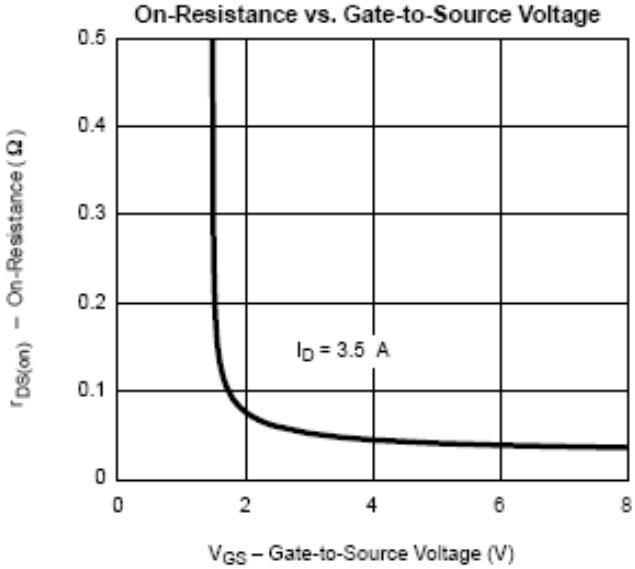
On-Resistance vs. Junction Temperature



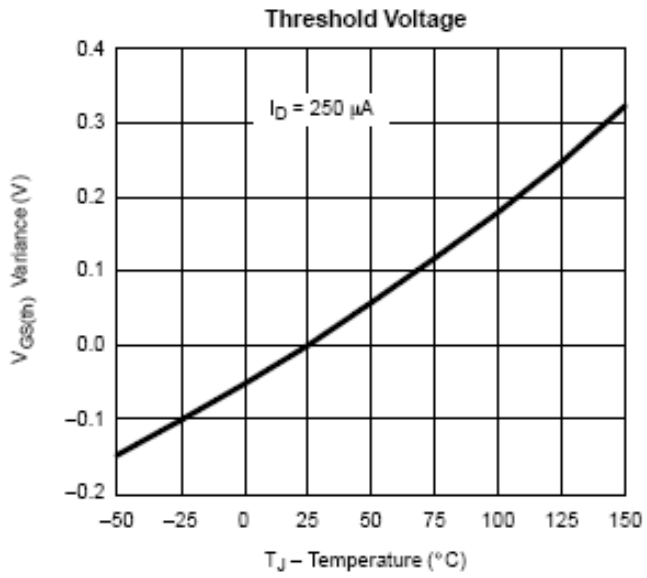
Source-Drain Diode Forward Voltage

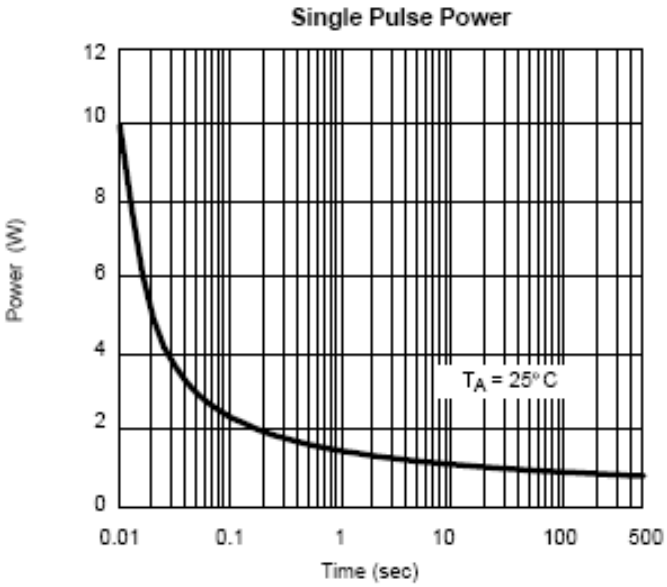


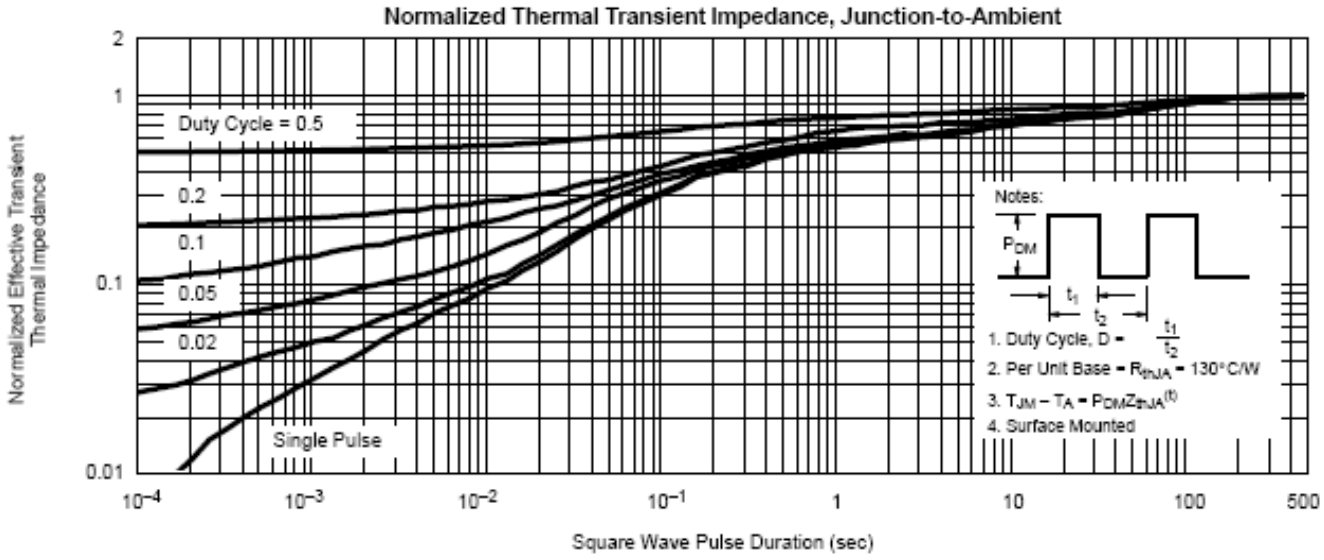
On-Resistance vs. Gate-to-Source Voltage



TYPICAL CHARACTERISTICS







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