SPP5413
P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP5413 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. The SPP5413 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

APPLICATIONS

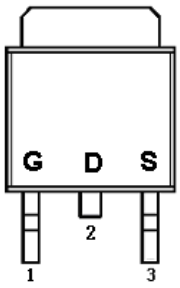
- Power Management in Note book
- Powered System
- DC/DC Converter
- Load Switch

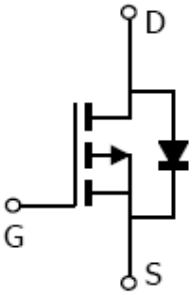
FEATURES

- -40V/-10A,$R_{DS(ON)}$=26mΩ@V_{GS}=-10V
- -40V/- 8A,$R_{DS(ON)}$=36mΩ@V_{GS}=-4.5V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-252-2L package design

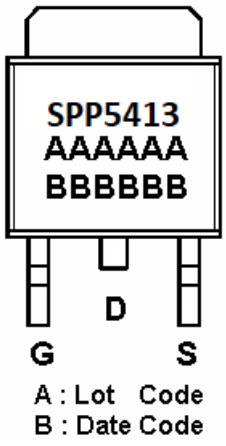
PIN CONFIGURATION

TO-252-2L





PART MARKING



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P-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP5413T252RGB	TO-252-2L	SPP5413

※ SPP5413T252RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-40	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	-18	A
	T_A=70℃		-10	
Pulsed Drain Current		I_{DM}	-30	A
Continuous Source Current(Diode Conduction)		I_S	-2.3	A
Power Dissipation	T_A=25℃	P_D	2.8	W
	T_A=70℃		1.8	
Avalanche Energy with Single Pulse (Tj=25℃, L = 0.14mH , I_{AS} = 43A , V_{DD} = 20V.)		E_{AS}	129	mJ
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	70	℃/W

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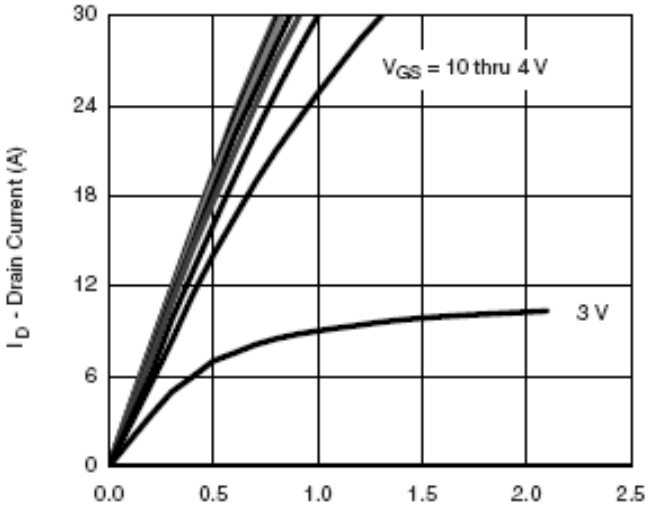
ELECTRICAL CHARACTERISTICS

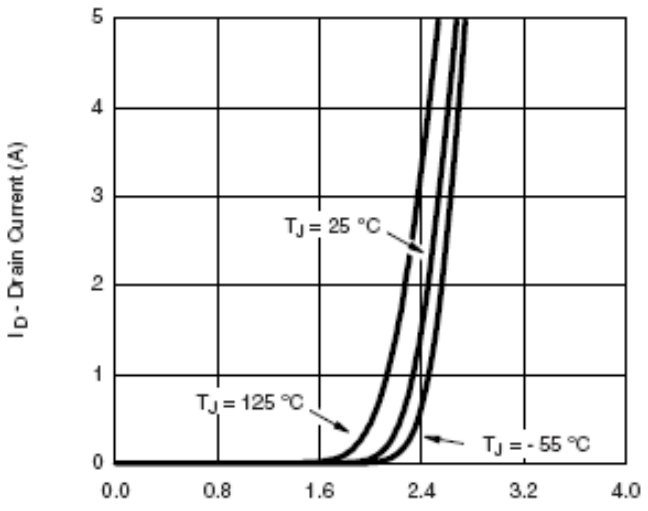
(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-40			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250uA	-0.8		-2.5	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-32V,V_{GS}=0V			-1	uA
		V_{DS}=-32V,V_{GS}=0V T_J=55℃			-10	
On-State Drain Current	$I_{D(on)}$	V_{DS}=-5V,V_{GS}=-4.5V	-10			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-10A		0.021	0.026	Ω
		V_{GS}=-4.5V,I_D=- 8A		0.030	0.036	
Forward Transconductance	gfs	V_{DS}=-15V,I_D=-5.7A		13		S
Diode Forward Voltage	V_{SD}	I_S=-2.3A,V_{GS}=0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-20V,V_{GS}=-4.5V I_D=-5.0A		13	20	nC
Gate-Source Charge	Q_{gs}			4.5		
Gate-Drain Charge	Q_{gd}			6.5		
Input Capacitance	C_{iss}	V_{DS}=-20V,V_{GS}=0V f=1MHz		1100		pF
Output Capacitance	C_{oss}			145		
Reverse Transfer Capacitance	C_{rss}			115		
Turn-On Time	$t_{d(on)}$	V_{DD}=-20V,R_L=4Ω I_D=-5.0A,V_{GEN}=-4.5V R_G=1Ω		40	80	nS
	t_r			55	100	
Turn-Off Time	$t_{d(off)}$			30	60	
	t_f			12	20	

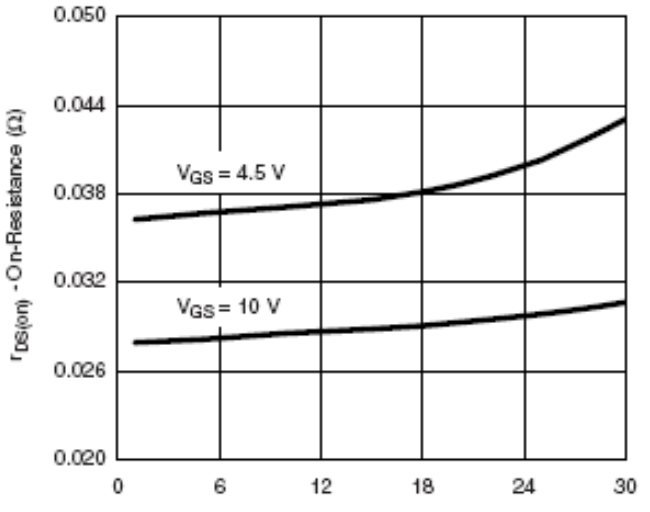
TYPICAL CHARACTERISTICS



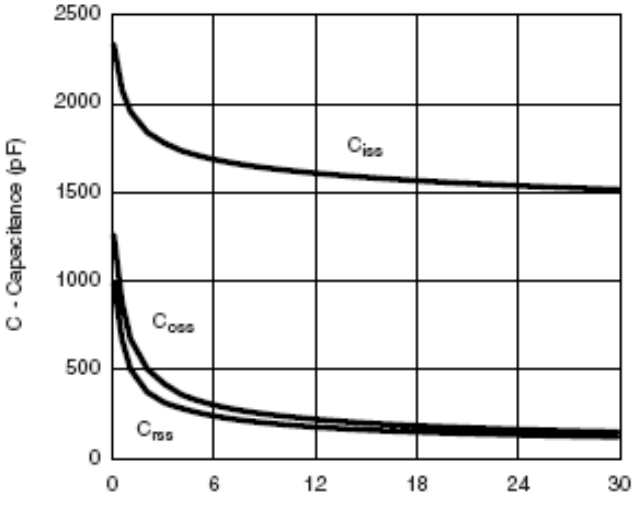
Output Characteristics



Transfer Characteristics

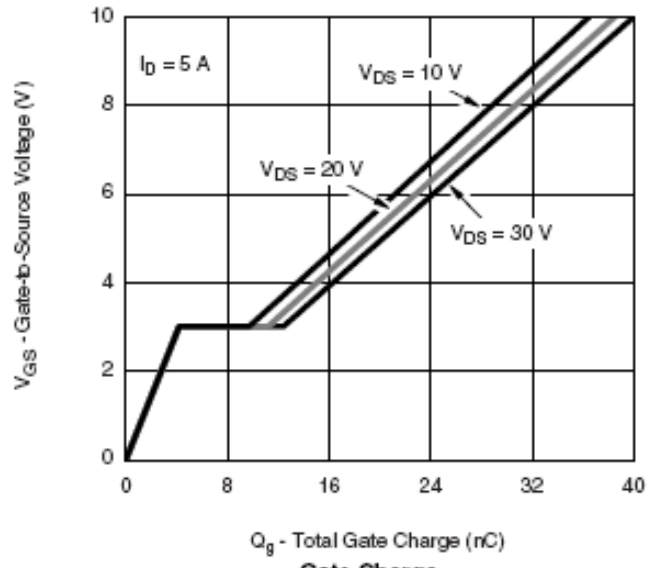


On-Resistance vs. Drain Current

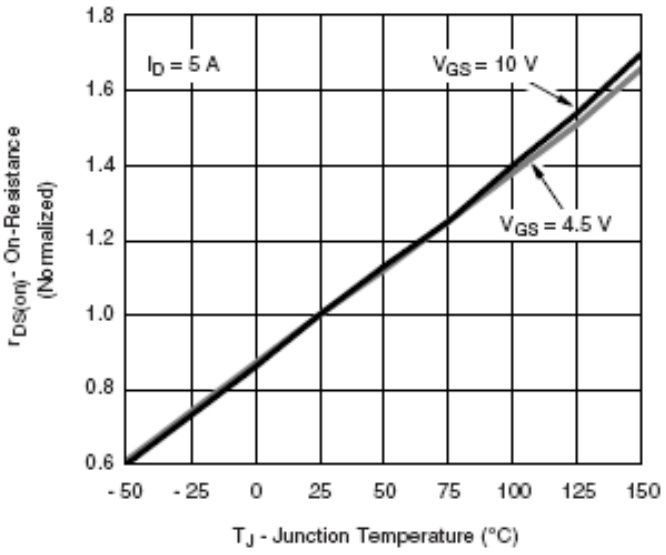


Capacitance

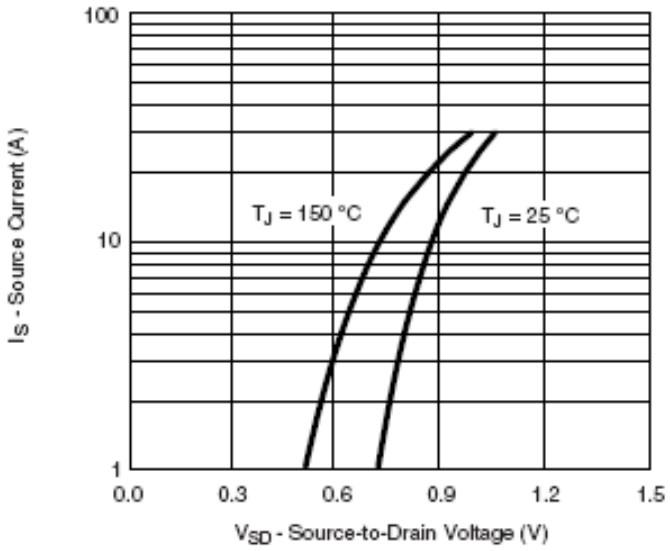
TYPICAL CHARACTERISTICS



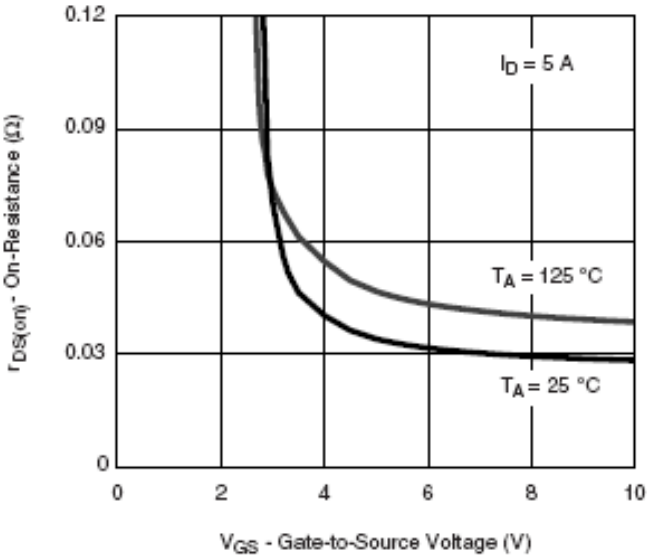
Gate Charge



On-Resistance vs. Junction Temperature

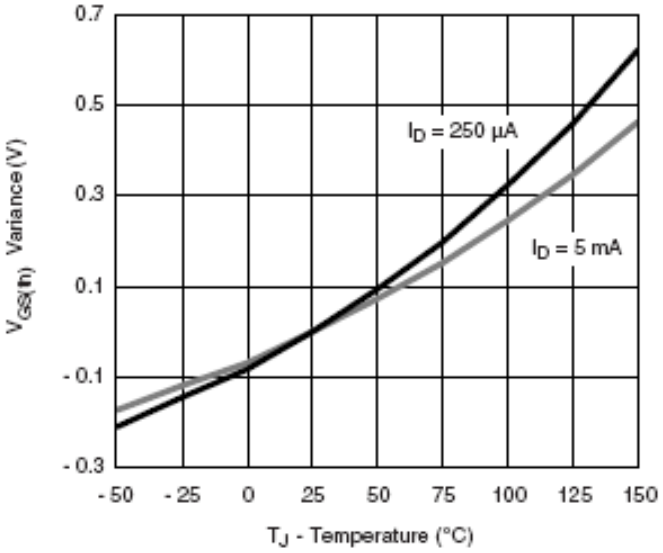


Source-Drain Diode Forward Voltage

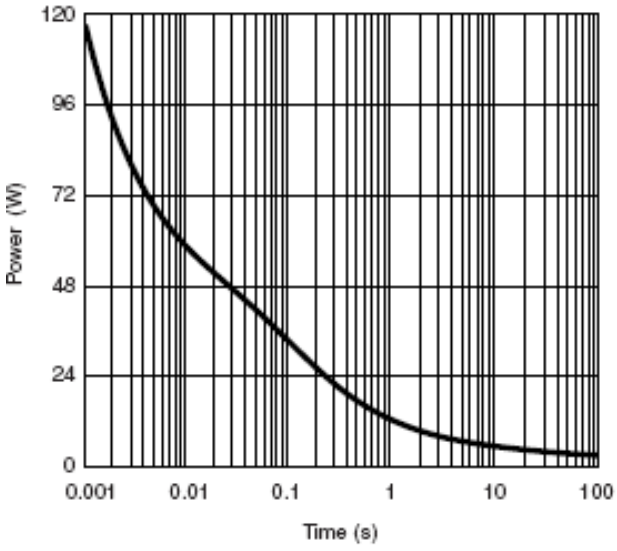


On-Resistance vs. Gate-to-Source Voltage

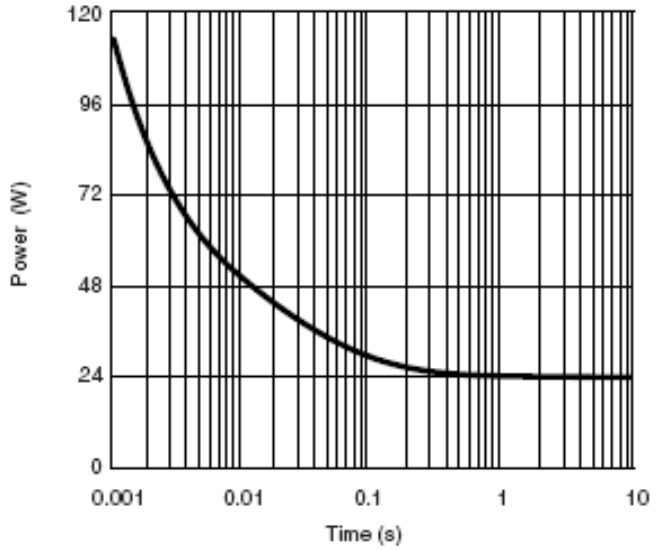
TYPICAL CHARACTERISTICS



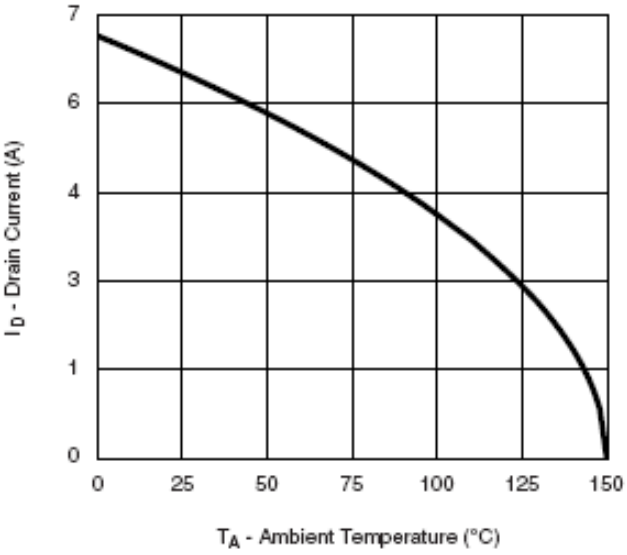
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

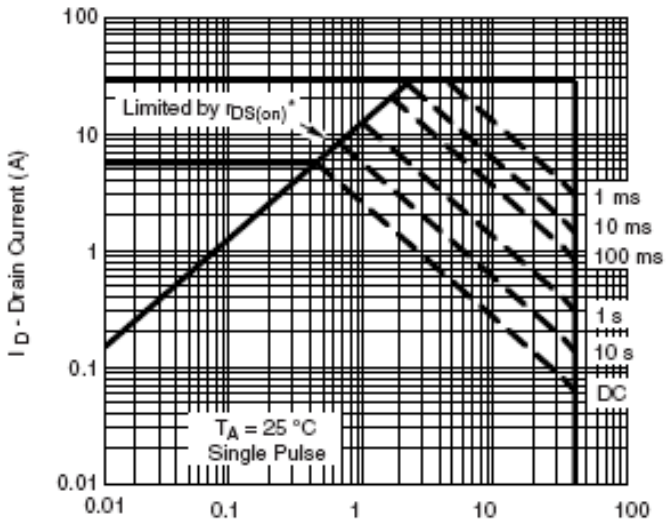


Single Pulse Power, Junction-to-Case

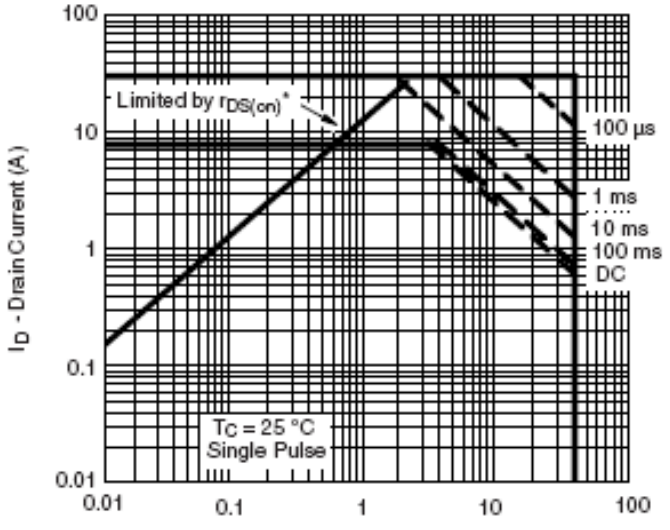


Current Derating*, Junction-to-Ambient

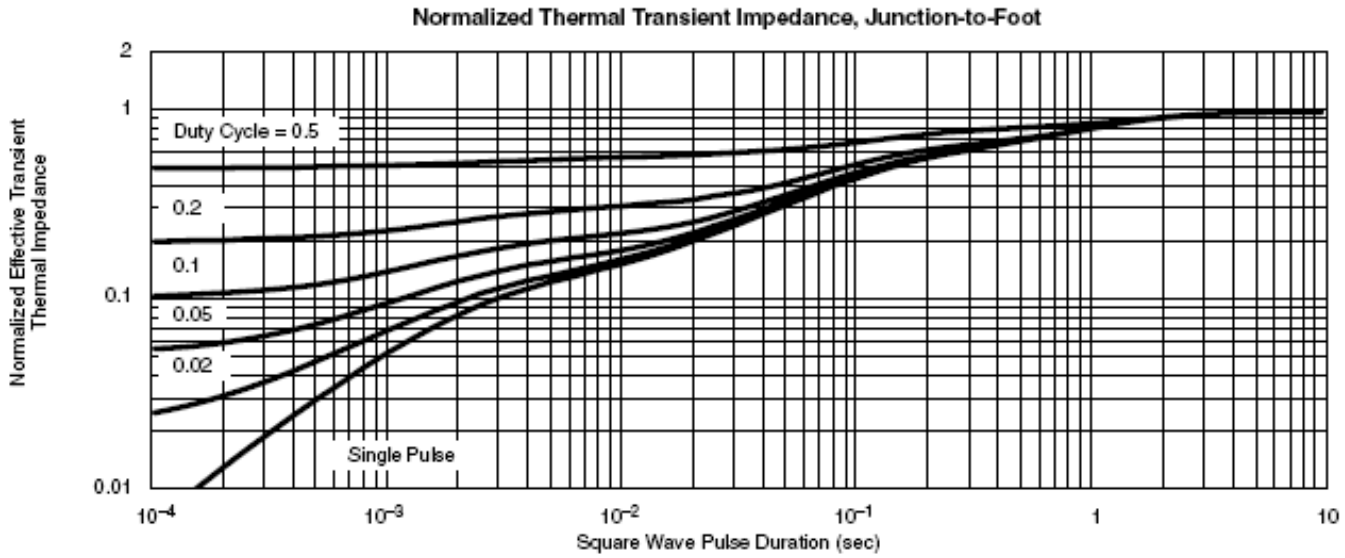
TYPICAL CHARACTERISTICS



Safe Operating Area, Junction-to-Ambient



Safe Operating Area, Junction-to-Case



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