



SPP3459

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP3459 is the P-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPP3459 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

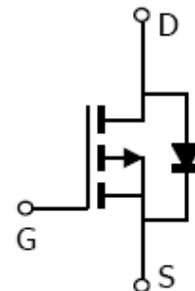
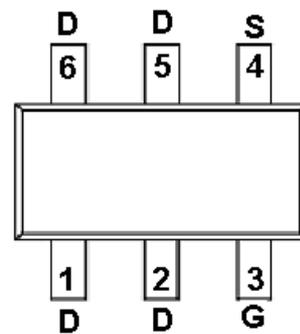
APPLICATIONS

- Powered System
- DC/DC Converter
- Load Switch

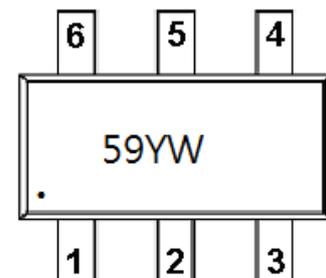
FEATURES

- ◆ -60V/-3A, $R_{DS(ON)}=140m\Omega@V_{GS}=-10V$
- ◆ -60V/-2A, $R_{DS(ON)}=190m\Omega@V_{GS}=-4.5V$
- ◆ High density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-23-6L package design

PIN CONFIGURATION(SOT-23-6L)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	D	Drain
2	D	Drain
3	G	Gate
4	S	Source
5	D	Drain
6	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP3459S26RGB	SOT-23-6L	59YW

※ SPP3459S26RGB : Tape Reel ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS (TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	-60	V	
Gate –Source Voltage	V _{GSS}	±20	V	
Continuous Drain Current(T _J =150°C)	I _D	TA=25°C	-3	A
		TA=70°C	-2.4	
Pulsed Drain Current	I _{DM}	-6	A	
Power Dissipation	P _D	TA=25°C	1.25	W
		TA=70°C	0.8	
Operating Junction Temperature	T _J	-55/150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	100	°C/W	



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ELECTRICAL CHARACTERISTICS (TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1		-2.5	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-48V, V_{GS}=0V,$ $T_J=25^\circ C$			1	uA
		$V_{DS}=-48V, V_{GS}=0V$ $T_J=55^\circ C$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS}=V_{GS}=0V$	-		-3	A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-3A$			140	mΩ
		$V_{GS}=-4.5V, I_D=-2A$			190	mΩ
Forward Transconductance	g_{fs}	$V_{DS}=-5V, I_D=-3A$		5.8		S
Diode Forward Voltage	V_{SD}	$I_S=-1A, V_{GS}=0V$			-1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-20V, V_{GS}=-4.5V$ $I_D=-3A$		5.9		nC
Gate-Source Charge	Q_{gs}			2.9		
Gate-Drain Charge	Q_{gd}			1.8		
Input Capacitance	C_{iss}	$V_{DS}=-15V, V_{GS}=0V$ $f=1MHz$		715		pF
Output Capacitance	C_{oss}			51		
Reverse Transfer Capacitance	C_{rss}			34		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-12V, I_D=-3A,$ $V_{GS}=-10V, R_G=3.3\Omega$		10		nS
	t_r			17		
Turn-Off Time	$t_{d(off)}$			22		
	t_f			21		



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TYPICAL CHARACTERISTICS

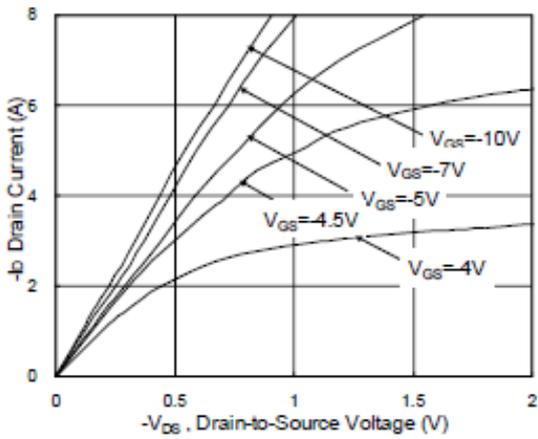


Fig.1 Typical Output Characteristics

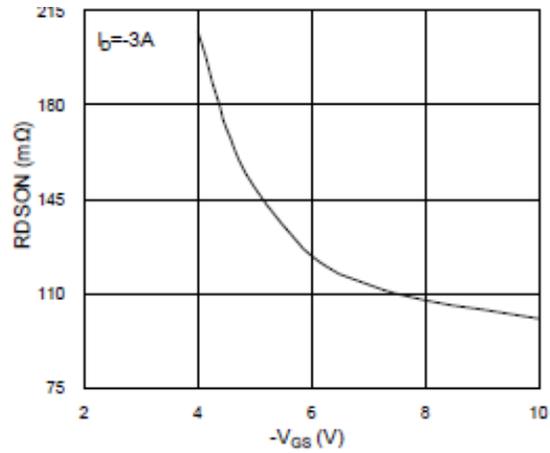


Fig.2 On-Resistance vs. G-S Voltage

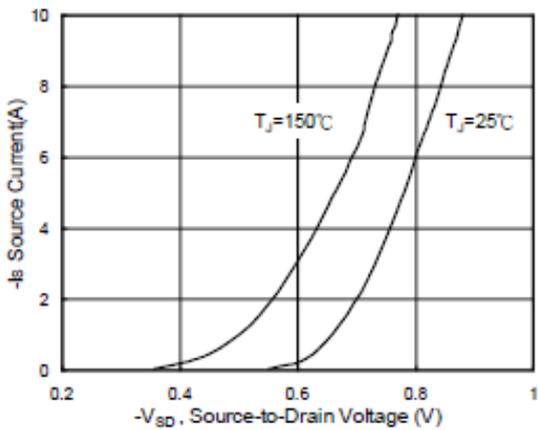


Fig.3 Forward Characteristics Of Reverse

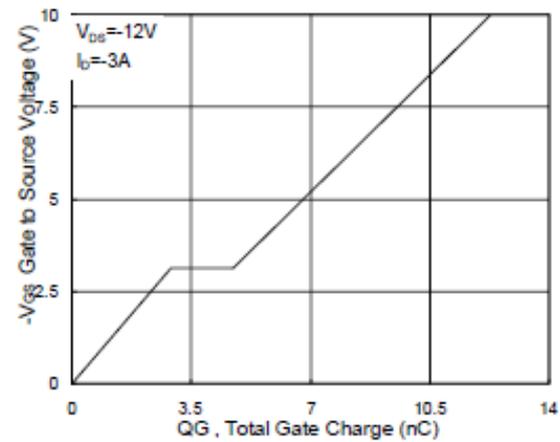


Fig.4 Gate-Charge Characteristics

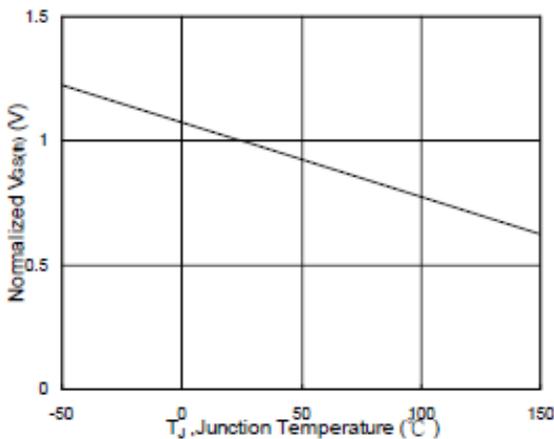


Fig.5 Normalized $V_{GS(th)}$ vs. T_j

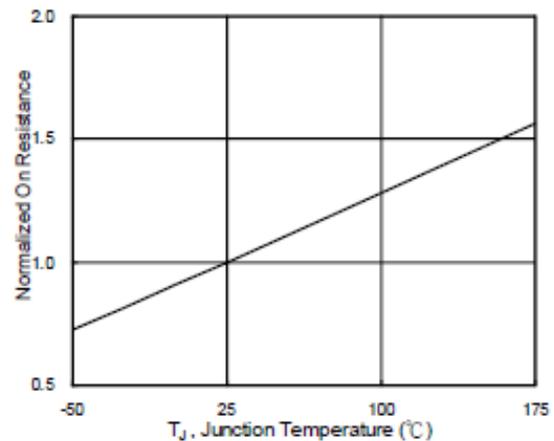


Fig.6 Normalized $R_{DS(on)}$ vs. T_j



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TYPICAL CHARACTERISTICS

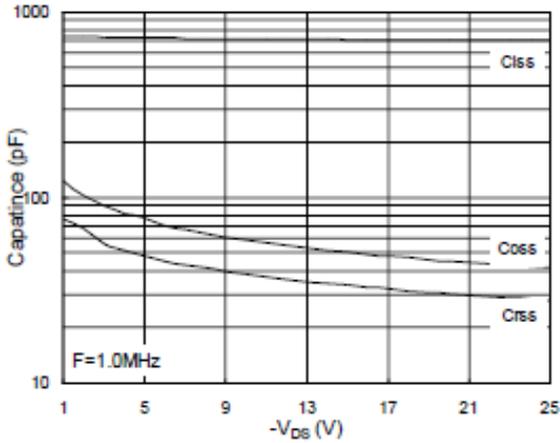


Fig.7 Capacitance

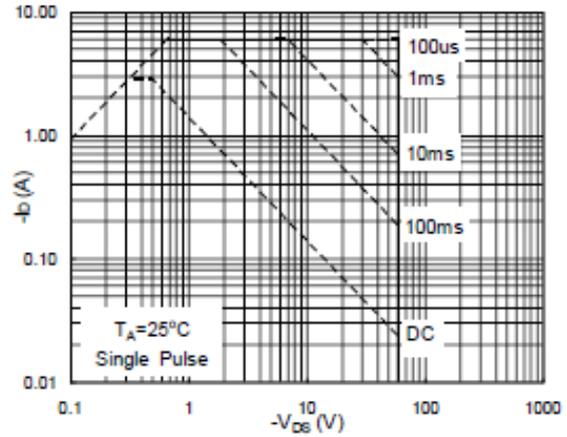


Fig.8 Safe Operating Area

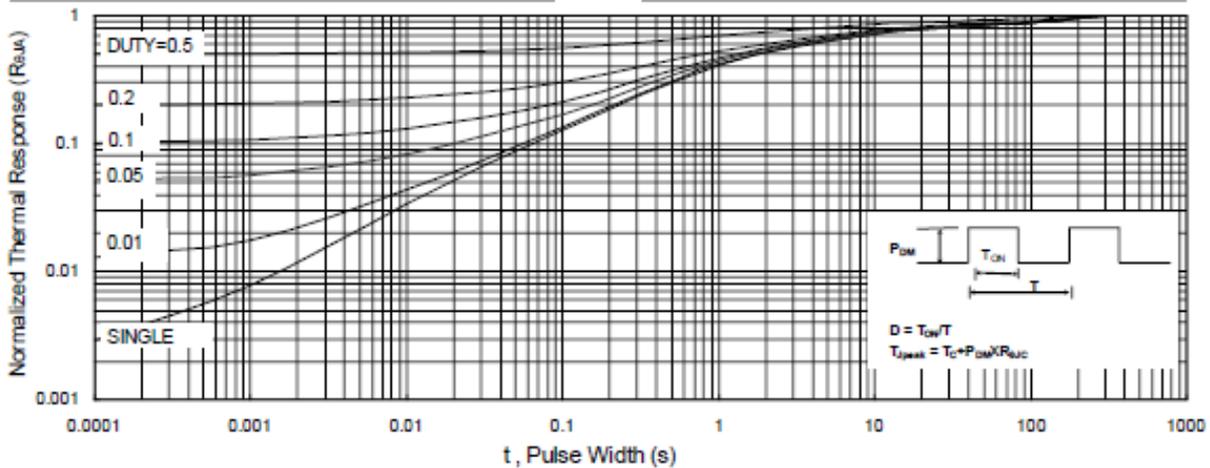


Fig.9 Normalized Maximum Transient Thermal Impedance

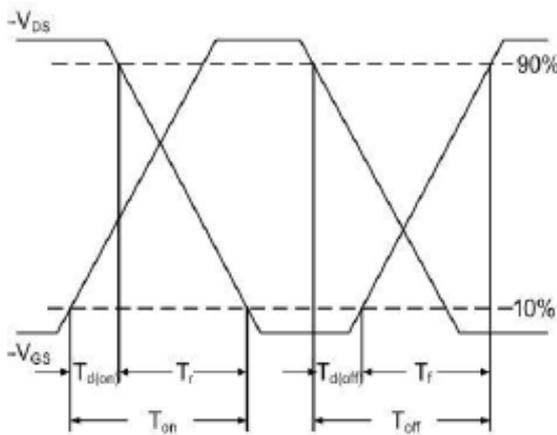


Fig.10 Switching Time Waveform

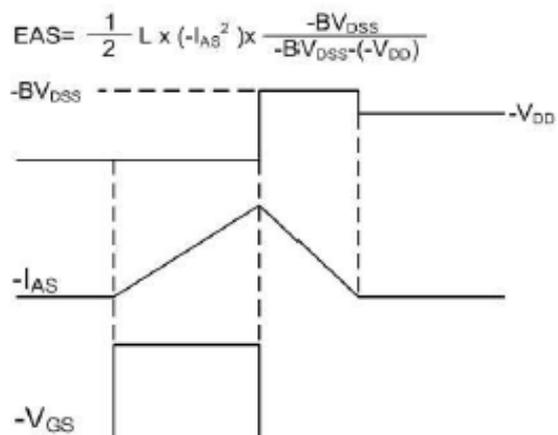


Fig.11 Unclamped Inductive Waveform



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