SPP3457
P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP3457 is the P-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPP3457 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

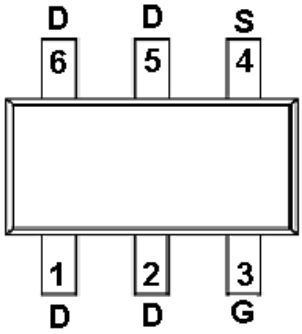
APPLICATIONS

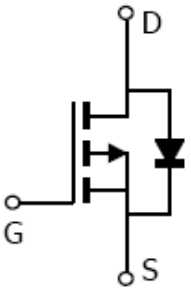
- Powered System
- DC/DC Converter
- Load Switch
- Battery Powered System

FEATURES

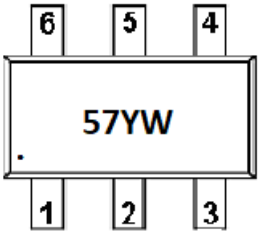
- -60V/-3.0A, $R_{DS(ON)}$=80mΩ@V_{GS}=-10V
- -60V/-2.7A, $R_{DS(ON)}$=100mΩ@V_{GS}=-4.5V
- High density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-6L package design

PIN CONFIGURATION(SOT-23-6L)





PART MARKING



Y : Year Code
W : Week Code

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PIN DESCRIPTION

Pin	Symbol	Description
1	D	Drain
2	D	Drain
3	G	Gate
4	S	Source
5	D	Drain
6	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP3457S26RGB	SOT-23-6L	57

※ SPP3457S26RGB : Tape Reel ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS (T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-60	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	-3.4	A
	T_A=70℃		-2.7	
Pulsed Drain Current		I_{DM}	-14	A
Power Dissipation	T_A=25℃	P_D	1.7	W
	T_A=70℃		1.1	
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	74	℃/W

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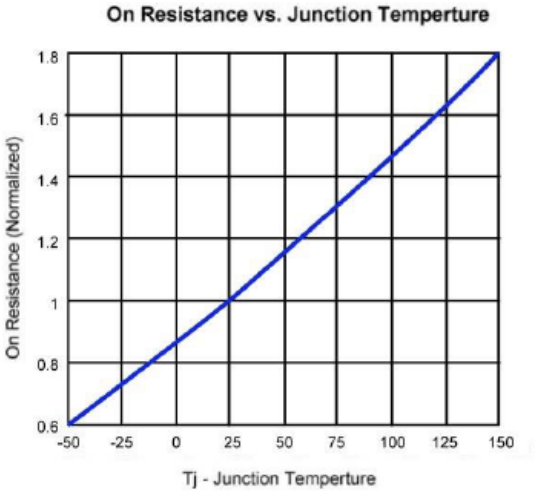
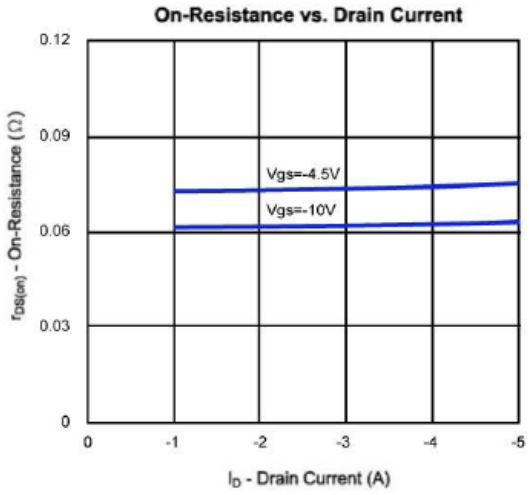
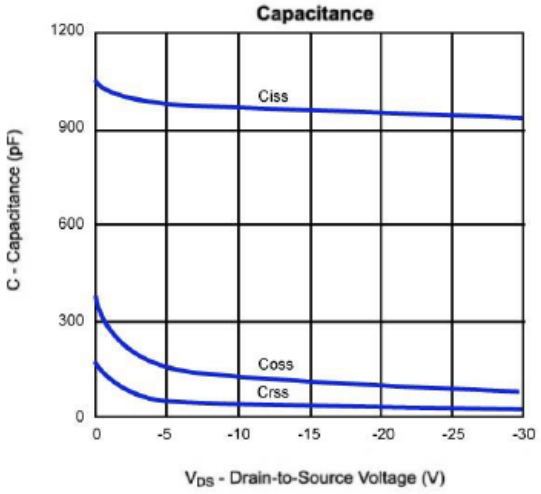
ELECTRICAL CHARACTERISTICS (T_A=25°C Unless otherwise noted)

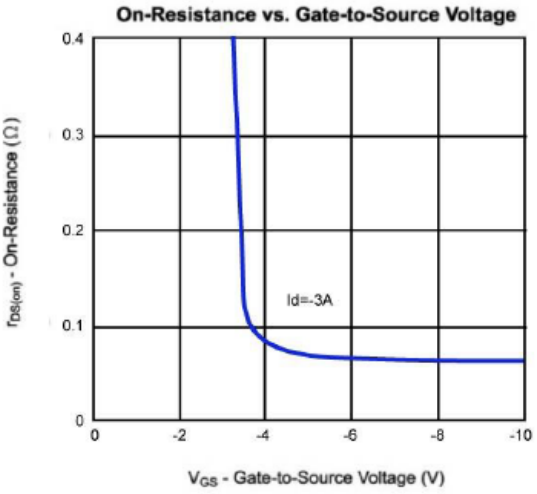
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250uA	-0.8		-3	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-48V,V_{GS}=0V, T_J=25°C			-1	uA
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-3A		65	80	mΩ
		V_{GS}=-4.5V,I_D=-2.7A		75	100	
Diode Forward Voltage	V_{SD}	I_S=-1.3A,V_{GS}=0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-30V,V_{GS}=-10V I_D=-3A		23		nC
Total Gate Charge	Q_g	V_{DS}=-30V,V_{GS}=-4.5V I_D=-3A		11.4		
Gate-Source Charge	Q_{gs}			4.8		
Gate-Drain Charge	Q_{gd}			4.6		
Input Capacitance	C_{iss}	V_{DS}=-15V,V_{GS}=0V f=1MHz		958		pF
Output Capacitance	C_{oss}			106		
Reverse Transfer Capacitance	C_{rss}			35		
Turn-On Time	$t_{d(on)}$	V_{DD}=-30V,R_L=30Ω, V_{GS}=-10V,R_G=6Ω		28		nS
	t_r			8		
Turn-Off Time	$t_{d(off)}$			62		
	t_f			9		

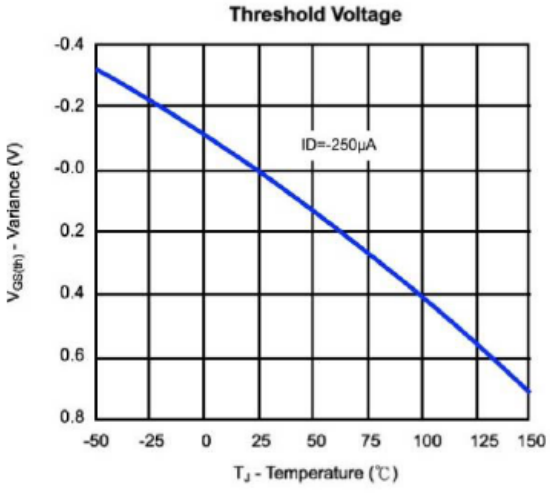
TYPICAL CHARACTERISTICS

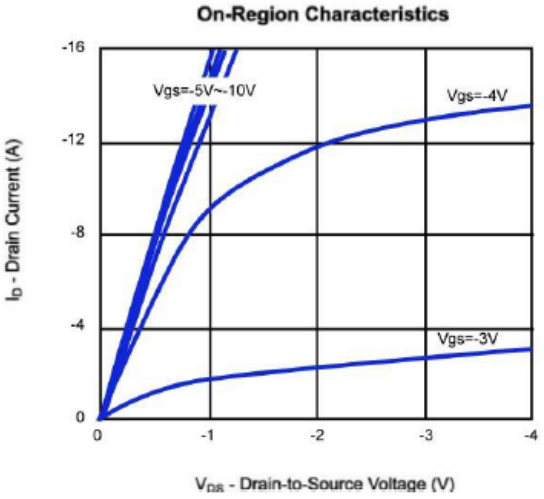






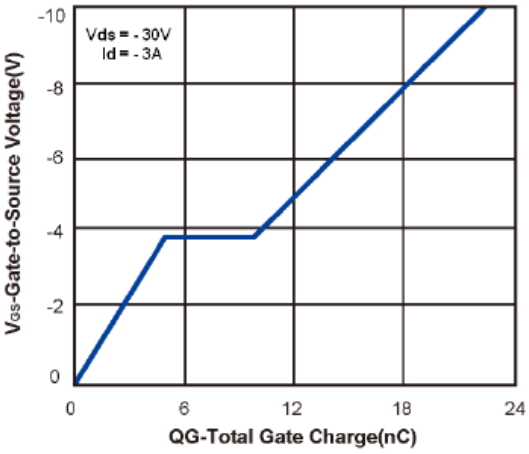




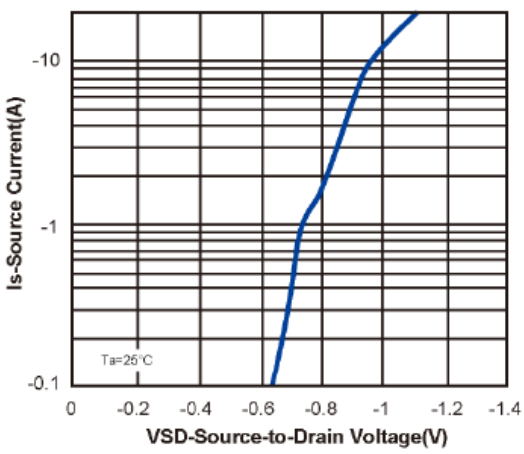


TYPICAL CHARACTERISTICS

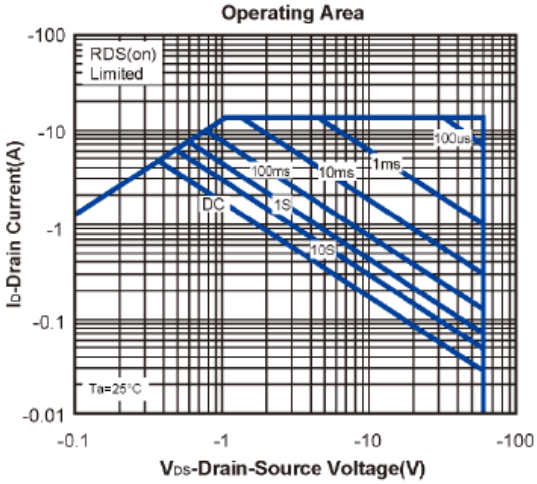
Gate Charge



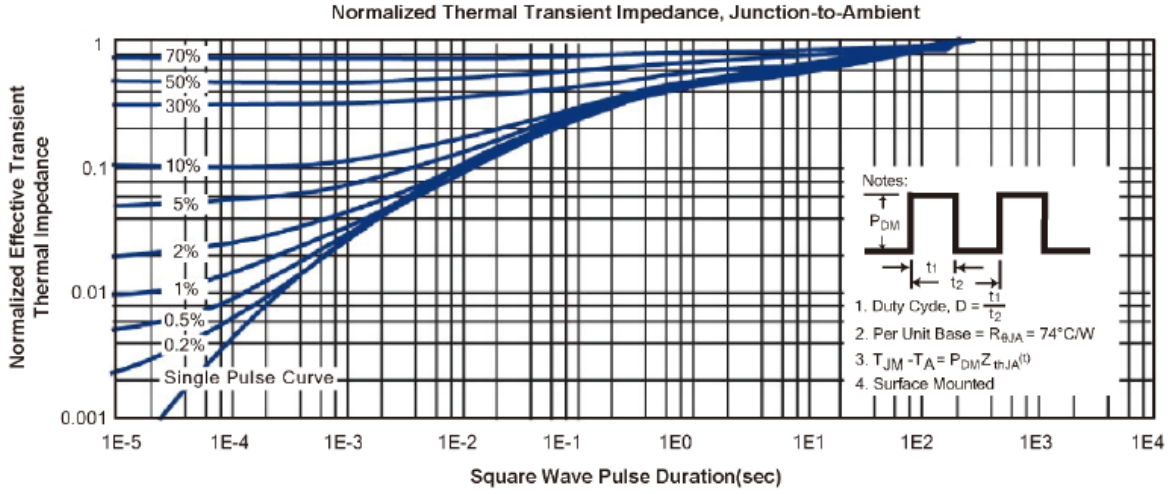
Body-diode characteristics



Maximum Forward Biased Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



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