



SPP3415

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP3415 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where high-side switching , and low in-line power loss are needed in a very small outline surface mount package.

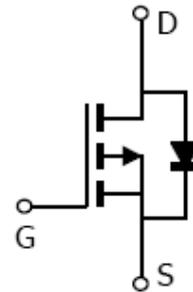
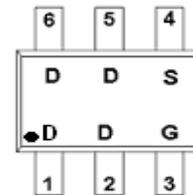
FEATURES

- ◆ -20V/-3.4A, $R_{DS(ON)}=130m\Omega@V_{GS}=-4.5V$
- ◆ -20V/-2.4A, $R_{DS(ON)}=150m\Omega@V_{GS}=-2.5V$
- ◆ -20V/-1.7A, $R_{DS(ON)}=190m\Omega@V_{GS}=-1.8V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-363 (SC-70-6L) package design

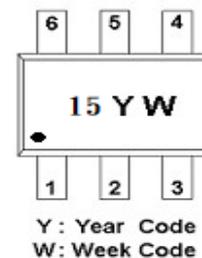
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION (SOT-363 / SC-70-6L)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
3	G	Gate
4	S	Source
1, 2, 5, 6	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP3415S36RGB	SOT-363	15

※ Week Code : A ~ Z (1 ~ 26) ; a ~ z (27 ~ 52)

※ SPP3415S36RGB : Tape Reel ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

($T_A=25^{\circ}\text{C}$ Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V_{DS}	-20	V	
Gate –Source Voltage	V_{GS}	± 12	V	
Continuous Drain Current($T_J=150^{\circ}\text{C}$)	I_D	$T_A=25^{\circ}\text{C}$	-2.3	A
		$T_A=70^{\circ}\text{C}$	-1.7	
Pulsed Drain Current	I_{DM}	-6	A	
Continuous Source Current(Diode Conduction)	I_S	-1.4	A	
Power Dissipation	P_D	$T_A=25^{\circ}\text{C}$	0.95	W
		$T_A=70^{\circ}\text{C}$	0.51	
Operating Junction Temperature	T_J	-55/150	$^{\circ}\text{C}$	
Storage Temperature Range	T_{STG}	-55/150	$^{\circ}\text{C}$	
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	105	$^{\circ}\text{C}/\text{W}$	



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ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

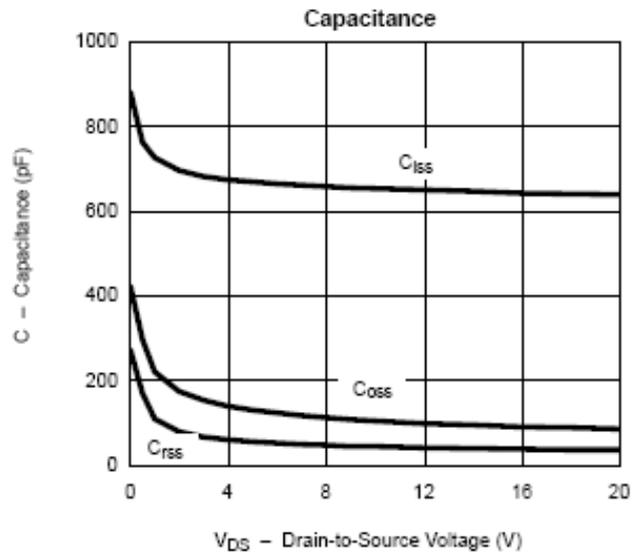
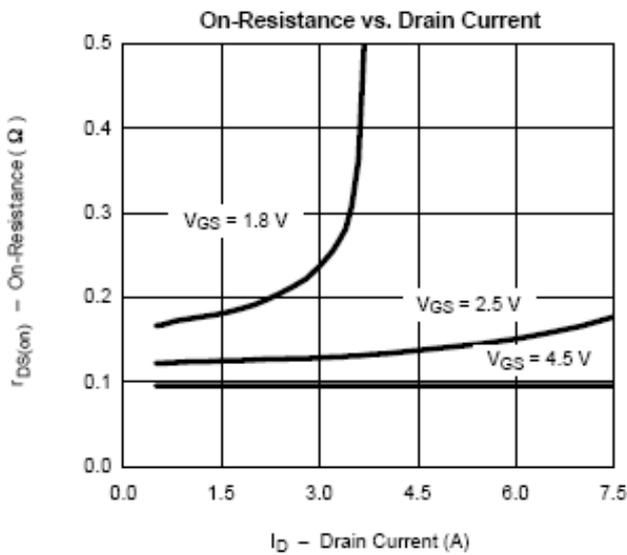
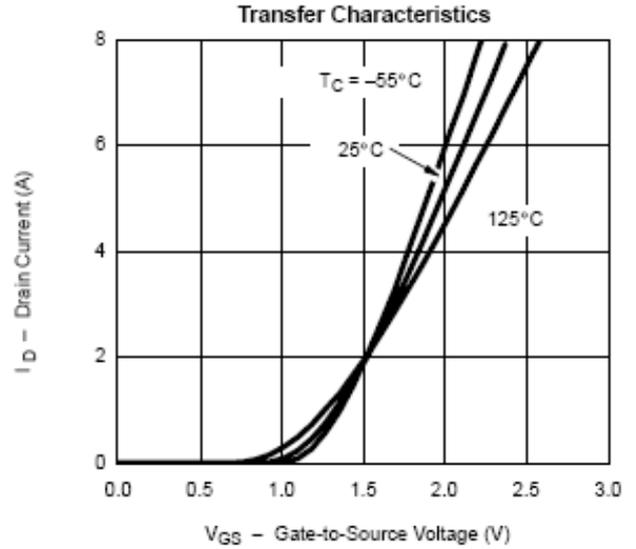
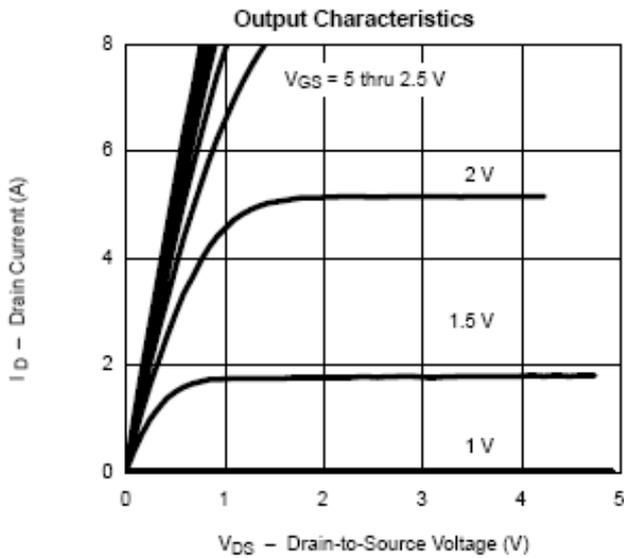
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =-250uA	-20			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-0.35		-0.8	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±12V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-20V, V _{GS} =0V			-1	uA
		V _{DS} =-20V, V _{GS} =0V T _J =55°C			-5	
On-State Drain Current	I _{D(on)}	V _{DS} ≤ -5V, V _{GS} =-4.5V	-6			A
Drain-Source On-Resistance	R _{Ds(on)}	V _{GS} =-4.5V, I _D =-3.4A		0.110	0.130	Ω
		V _{GS} =-2.5V, I _D =-2.4A		0.130	0.150	
		V _{GS} =-1.8V, I _D =-1.7A		0.170	0.190	
Forward Transconductance	g _{fs}	V _{DS} =-5V, I _D =-2.8A		6		S
Diode Forward Voltage	V _{SD}	I _S =-1.5A, V _{GS} =0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =-6V, V _{GS} =-4.5V I _D =-2.8A		4.8	8	nC
Gate-Source Charge	Q _{gs}			1.0		
Gate-Drain Charge	Q _{gd}			1.0		
Input Capacitance	C _{iss}	V _{DS} =-6V, V _{GS} =0V f=1MHz		485		pF
Output Capacitance	C _{oss}			85		
Reverse Transfer Capacitance	C _{rss}			40		
Turn-On Time	t _{d(on)}	V _{DD} =-6V, R _L =6Ω I _D =-1.0A, V _{GEN} =-4.5V R _G =6Ω		10	16	nS
	t _r			13	23	
Turn-Off Time	t _{d(off)}			18	25	
	t _f			15	20	



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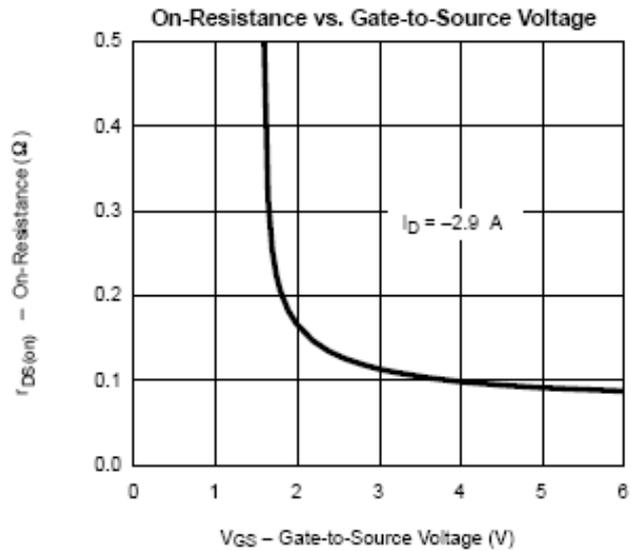
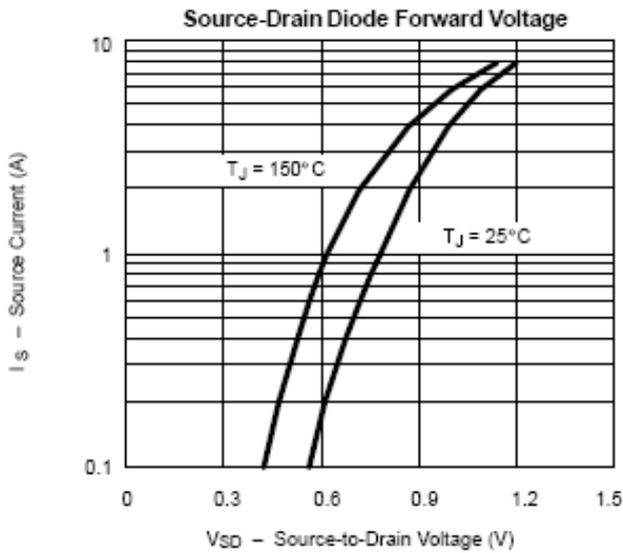
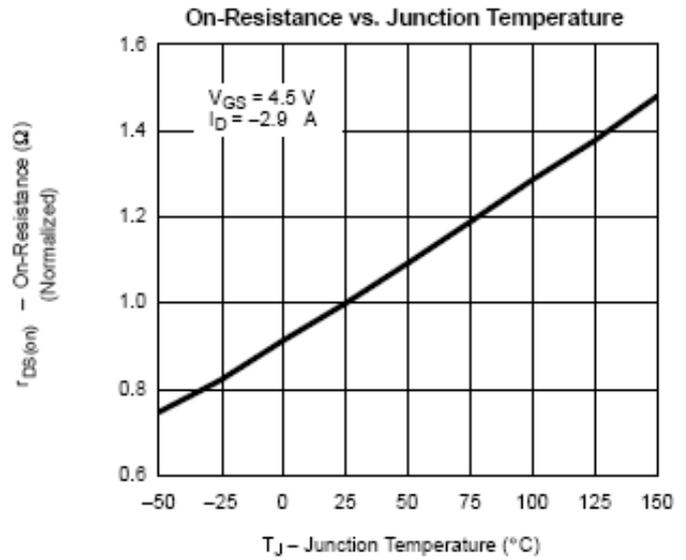
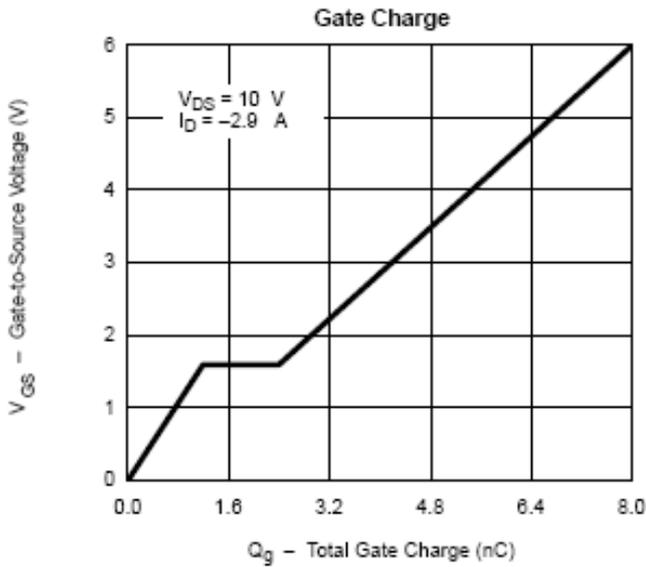
TYPICAL CHARACTERISTICS





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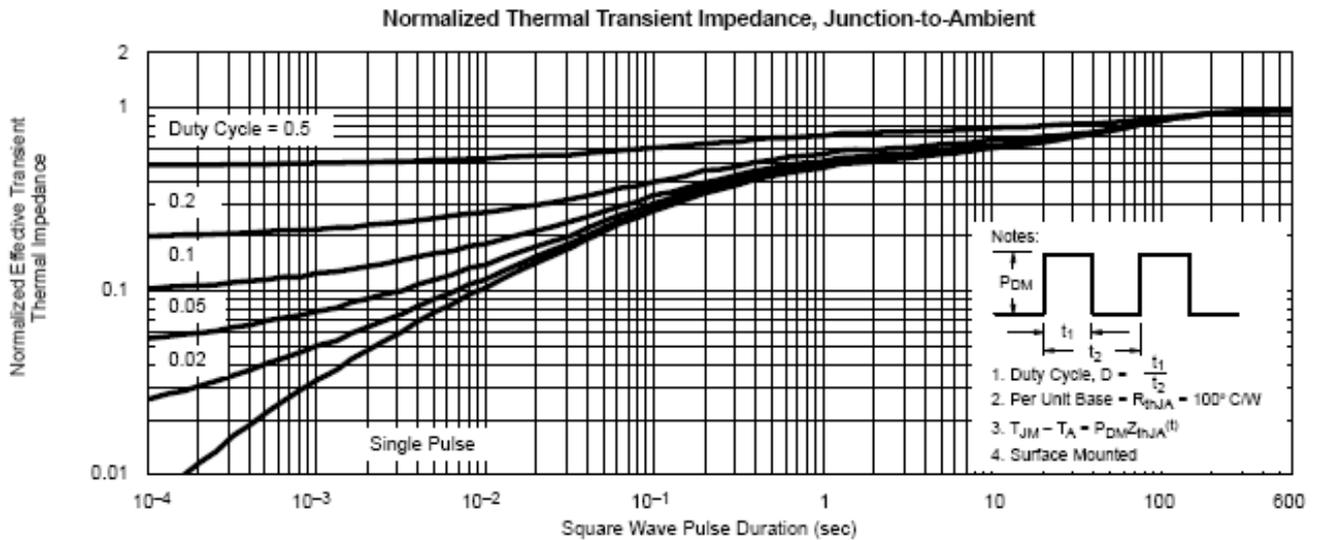
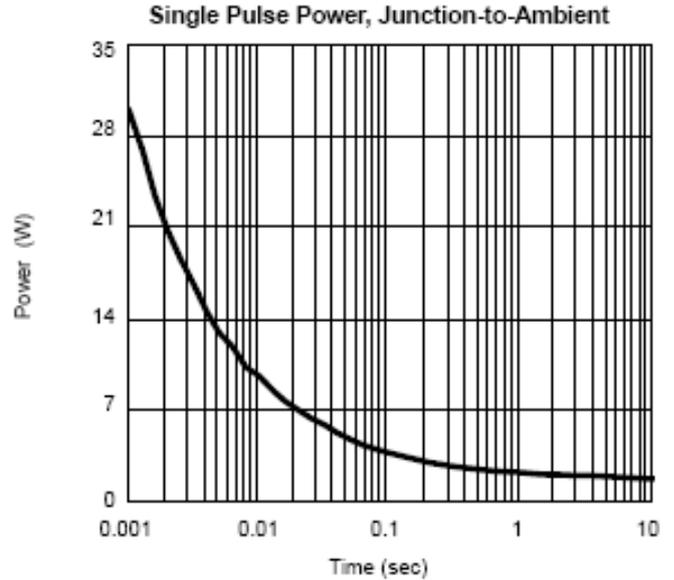
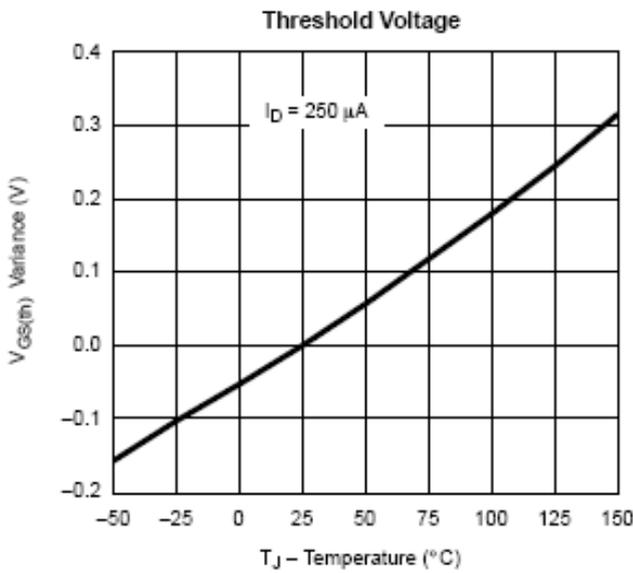




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TYPICAL CHARACTERISTICS





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