



SPP3095

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP3095 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, such as DC/DC converter and Desktop computer power management.

The package is universally preferred for commercial industrial surface mount applications

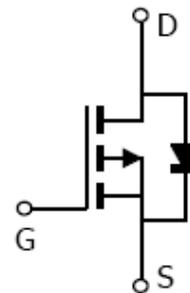
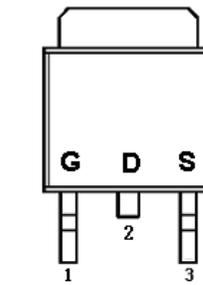
FEATURES

- ◆ -30V/-8A, $R_{DS(ON)}=100m\Omega@V_{GS}=-10V$
- ◆ -30V/-6A, $R_{DS(ON)}=150m\Omega@V_{GS}=-4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TO-252-2L package design

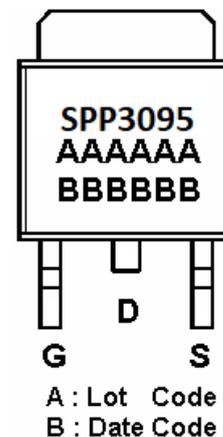
APPLICATIONS

- Power Management in Desktop Computer
- DC/DC Converter
- LCD Display inverter

PIN CONFIGURATION (TO-252-2L)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP3095T252RGB	TO-252-2L	SPP3095

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)

※ SPP3095T252RGB : Tape Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	-30	V	
Gate –Source Voltage	V _{GSS}	±20	V	
Continuous Drain Current(T _J =150°C)	I _D	TA=25°C	-12	A
		TA=70°C	-8	
Pulsed Drain Current	I _{DM}	-20	A	
Continuous Source Current(Diode Conduction)	I _S	-2.3	A	
Power Dissipation	P _D	TA=25°C	2.8	W
		TA=70°C	1.8	
Operating Junction Temperature	T _J	-55/150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	105	°C/W	



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ELECTRICAL CHARACTERISTICS

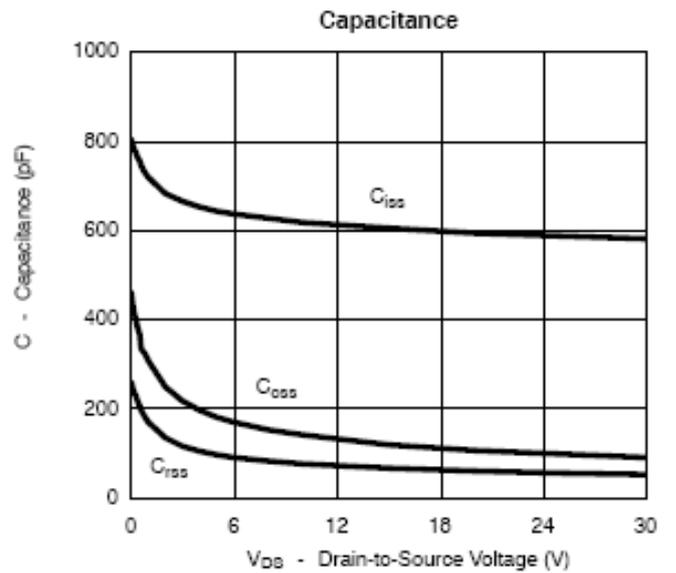
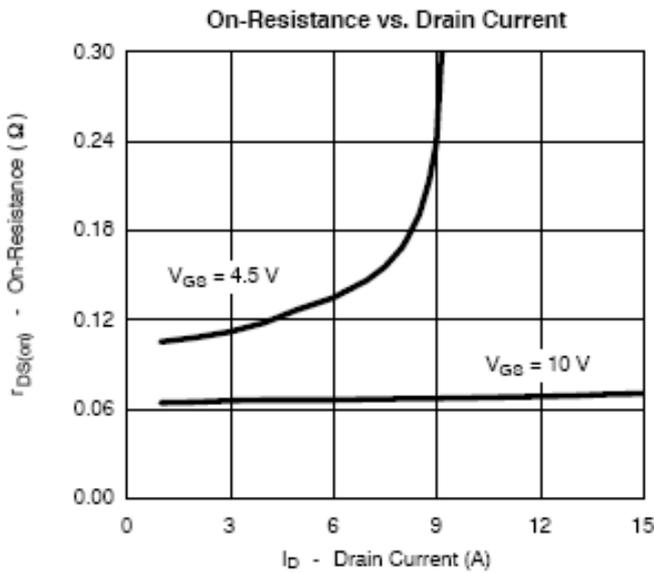
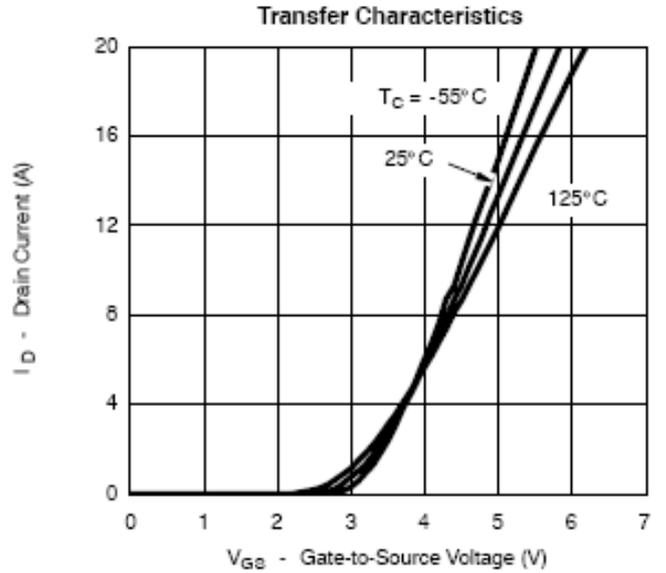
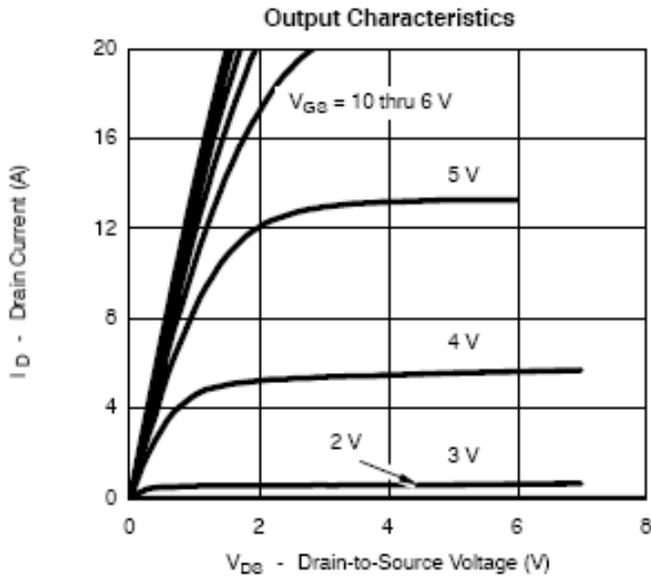
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Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=-250\mu A$	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0		-3.0	V
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-24V, V_{GS}=0V$			-1	uA
		$V_{DS}=-24V, V_{GS}=0V$ $T_J=85^\circ C$			-5	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=-10V, I_D=-8A$		0.083	0.100	Ω
		$V_{GS}=-4.5V, I_D=-6A$		0.130	0.150	
Forward Transconductance	g_{fs}	$V_{DS}=-10V, I_D=-8A$		8		S
Diode Forward Voltage	V_{SD}	$I_S=-2.5A, V_{GS}=0V$		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-15V, V_{GS}=-10V$ $I_D=-8A$		5.8	10	nC
Gate-Source Charge	Q_{gs}			0.8		
Gate-Drain Charge	Q_{gd}			1.5		
Input Capacitance	C_{iss}	$V_{DS}=-15V, V_{GS}=0V$ $f=1MHz$		226		pF
Output Capacitance	C_{oss}			87		
Reverse Transfer Capacitance	C_{rss}			19		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-15V, R_L=15\Omega$ $I_D=-1.0A, V_{GEN}=-10V$ $R_G=6\Omega$		9	20	nS
	t_r			9	20	
Turn-Off Time	$t_{d(off)}$			18	35	
	t_f			6	20	



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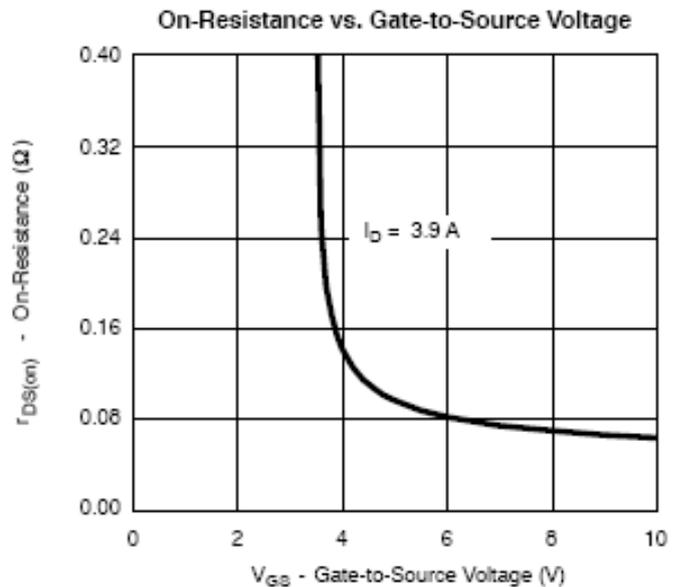
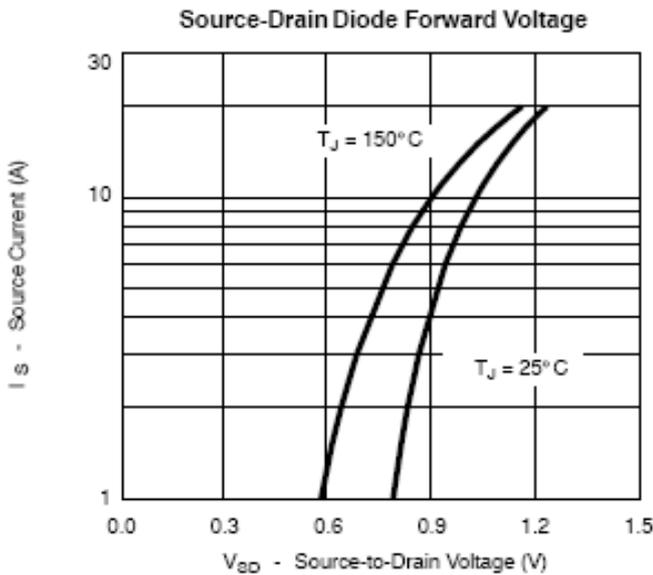
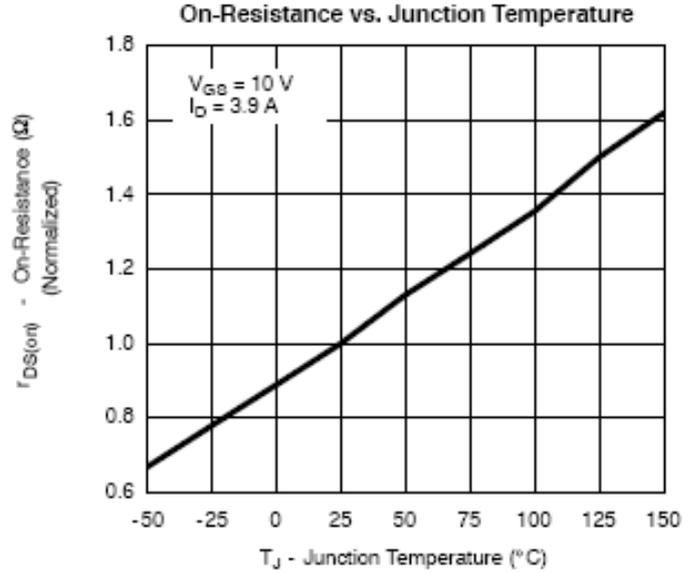
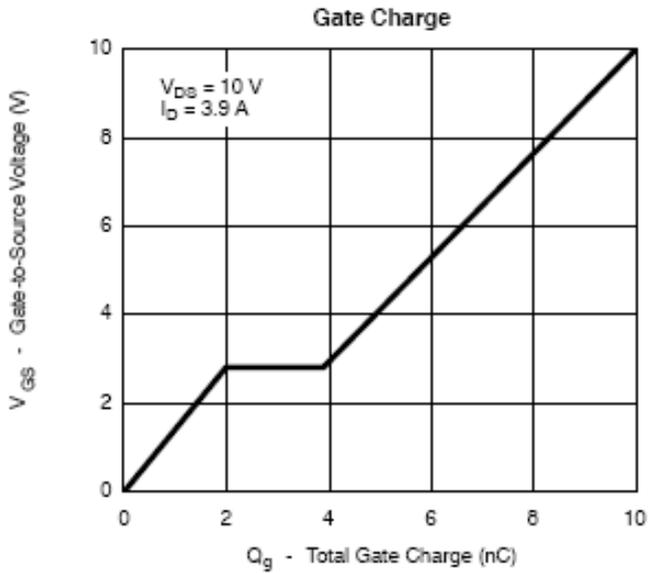
TYPICAL CHARACTERISTICS





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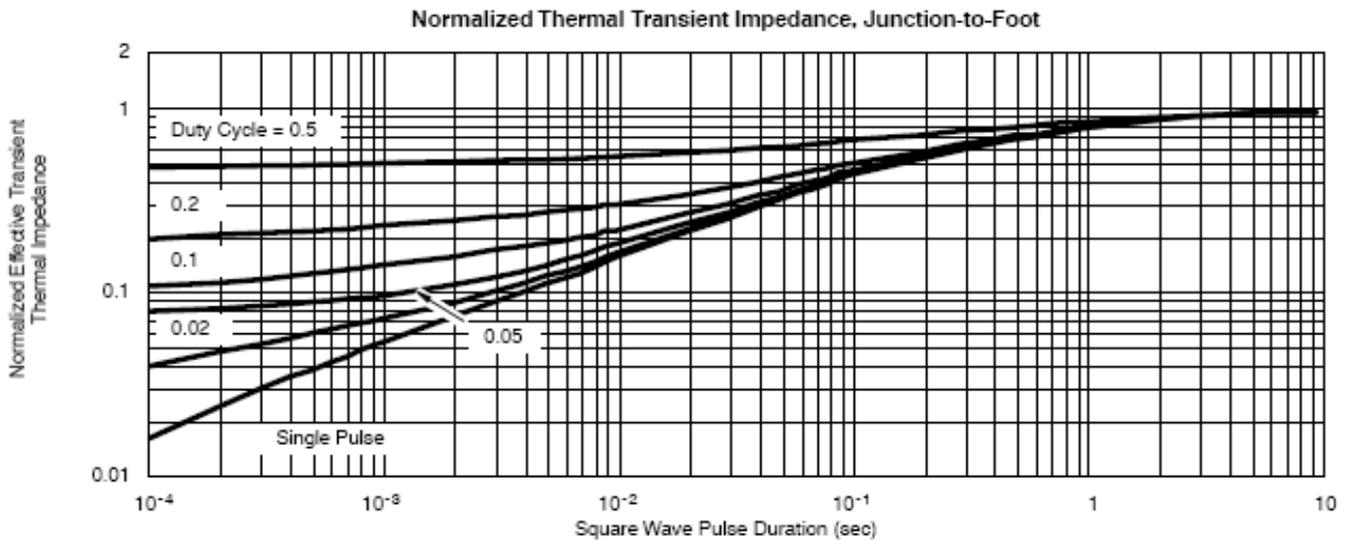
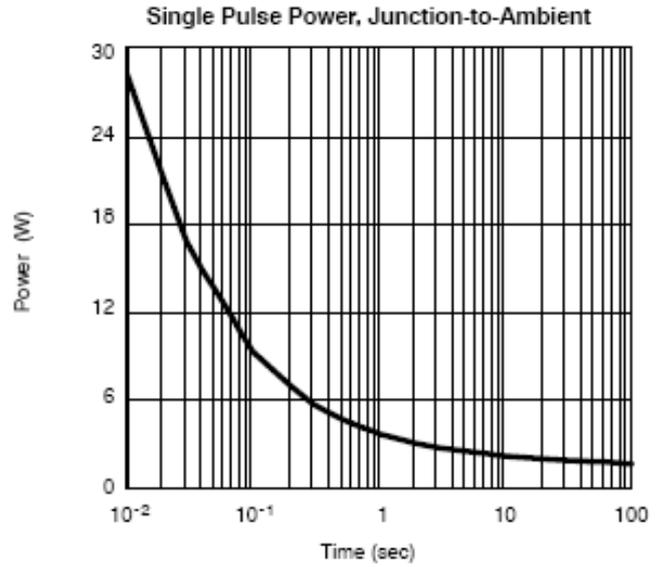
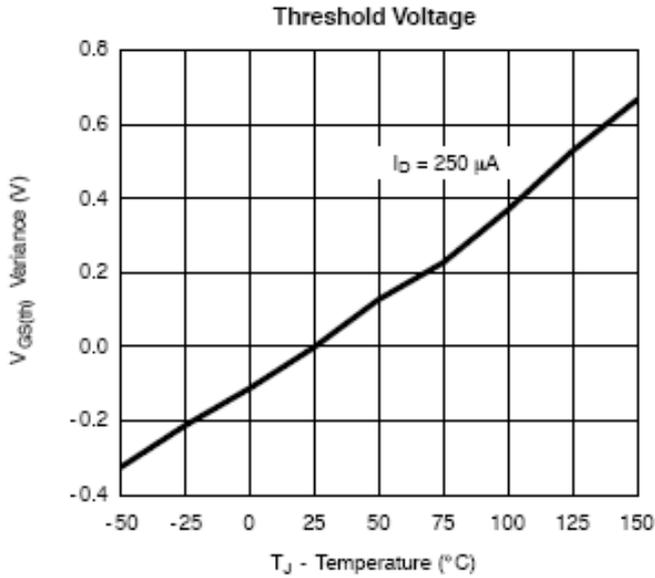
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