



# SPP2329

## P-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPP2329 is the P-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPP2329 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $R_{DS(ON)}$  and fast switching speed.

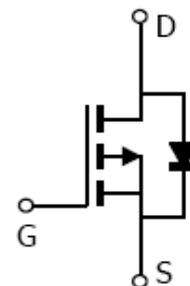
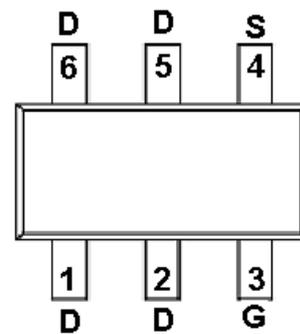
### APPLICATIONS

- Powered System
- DC/DC Converter
- Load Switch

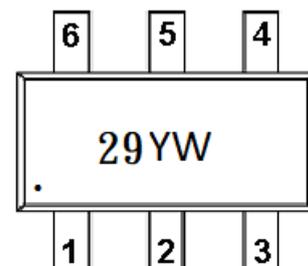
### FEATURES

- ◆  $-150V/-1.0A$ ,  $R_{DS(ON)}=900m\Omega@V_{GS}=-10V$
- ◆  $-150V/-1.0A$ ,  $R_{DS(ON)}=1000m\Omega@V_{GS}=-4.5V$
- ◆ High density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-23-6L package design

### PIN CONFIGURATION(SOT-23-6L)



### PART MARKING





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### PIN DESCRIPTION

Pin	Symbol	Description
1	D	Drain
2	D	Drain
3	G	Gate
4	S	Source
5	D	Drain
6	D	Drain

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPP2329S26RGB	SOT-23-6L	29

※ SPP2329S26RGB : Tape Reel ; Pb – Free ; Halogen – Free

### ABSOLUTE MAXIMUM RATINGS (TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V <sub>DSS</sub>	-150	V
Gate –Source Voltage	V <sub>GSS</sub>	±20	V
Continuous Drain Current	I <sub>D</sub>	-1.0	A
Pulsed Drain Current *Note1	I <sub>DM</sub>	-3.0	A
Power Dissipation	P <sub>D</sub>	2.1	W
Operating Junction Temperature	T <sub>J</sub>	-55/150	°C
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C
Thermal Resistance-Junction to Ambient *Note2	R <sub>θJA</sub>	60	°C/W

Notes:

1. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
2. R<sub>θJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design. R<sub>θJA</sub> shown below for single device operation on FR-4 in still air.



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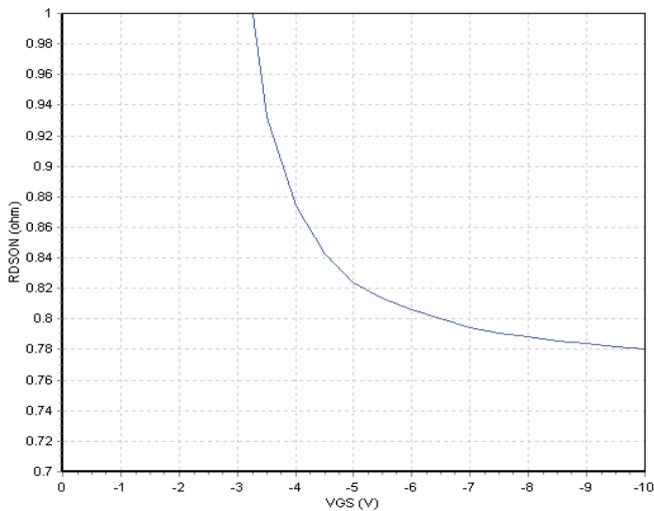
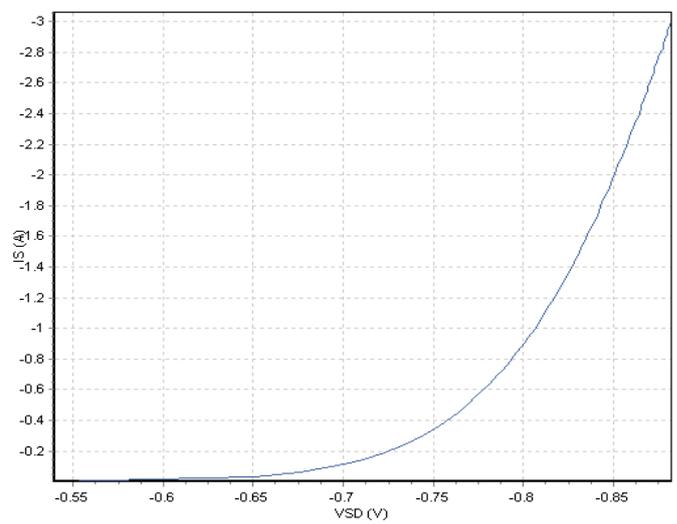
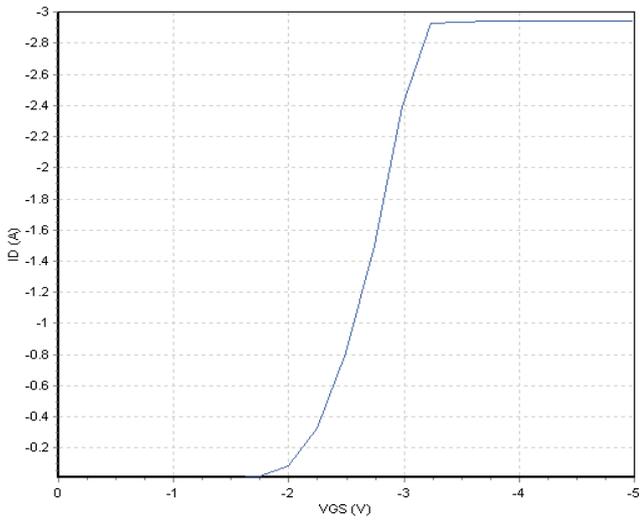
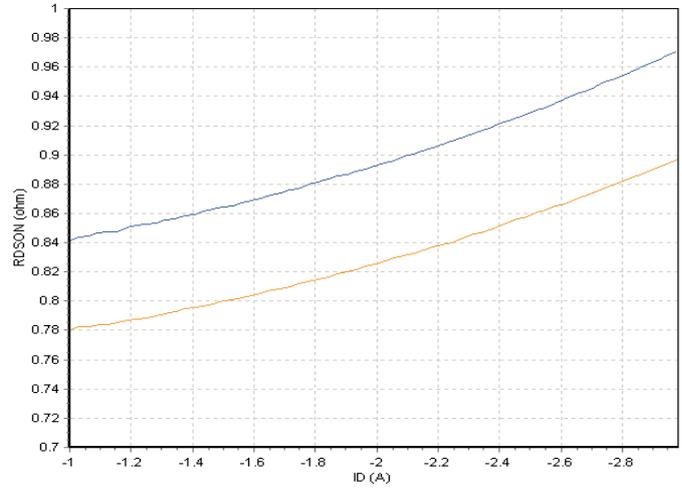
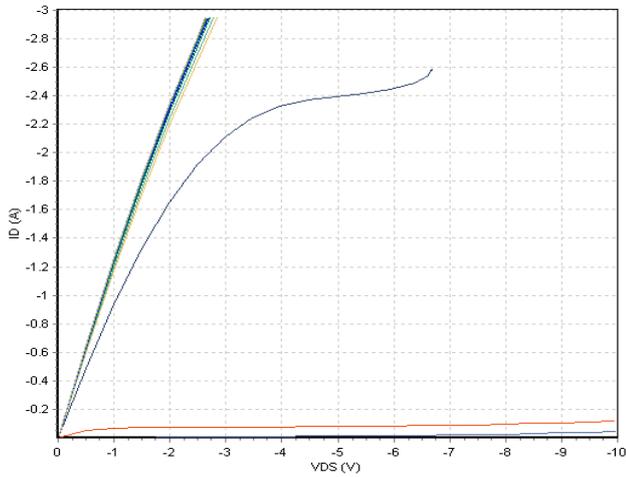
### ELECTRICAL CHARACTERISTICS (TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-150			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250uA	-1		-3.0	
Gate Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-120V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C			-1	uA
On-State Drain Current	I <sub>D(on)</sub>	V <sub>DS</sub> =V <sub>GS</sub> =0V			-1.0	A
Drain-Source On-Resistance	R <sub>DSS(on)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-1A		780	900	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-1A		880	1000	mΩ
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> =-10V, I <sub>D</sub> =-1A		2.4		S
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-1A, V <sub>GS</sub> =0V	-0.4		-1.0	V
<b>Dynamic</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-75V, V <sub>GS</sub> =-10V I <sub>D</sub> =-1A		20		nC
Gate-Source Charge	Q <sub>gs</sub>			5		
Gate-Drain Charge	Q <sub>gd</sub>			8		
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-75, V <sub>GS</sub> =0V f=1MHz		750		pF
Output Capacitance	C <sub>oss</sub>			48		
Reverse Transfer Capacitance	C <sub>rss</sub>			20		
Turn-On Time	t <sub>d(on)</sub>	V <sub>DD</sub> =-75V, V <sub>GS</sub> =-10V, R <sub>G</sub> =3.0Ω		12		nS
	t <sub>r</sub>			32		
Turn-Off Time	t <sub>d(off)</sub>			30		
	t <sub>f</sub>			10		



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## TYPICAL CHARACTERISTIC





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