SPP2329
P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP2329 is the P-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPP2329 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

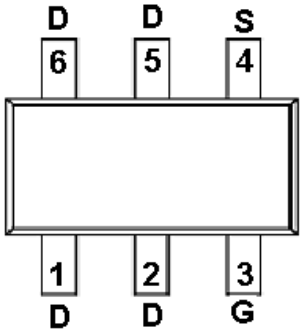
APPLICATIONS

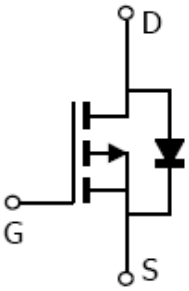
- Powered System
- DC/DC Converter
- Load Switch

FEATURES

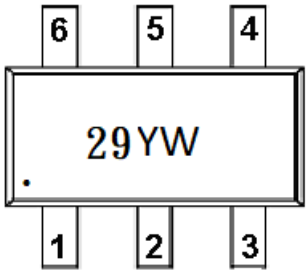
- -150V/-1.0A, $R_{DS(ON)}$=900mΩ@V_{GS}=-10V
- -150V/-1.0A, $R_{DS(ON)}$=1000mΩ@V_{GS}=-4.5V
- High density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-6L package design

PIN CONFIGURATION(SOT-23-6L)





PART MARKING



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PIN DESCRIPTION

Pin	Symbol	Description
1	D	Drain
2	D	Drain
3	G	Gate
4	S	Source
5	D	Drain
6	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP2329S26RGB	SOT-23-6L	29

※ SPP2329S26RGB : Tape Reel ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS (T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	-150	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current	T_A=25℃	I_D	-1.0	A
Pulsed Drain Current *Note1		I_{DM}	-3.0	A
Power Dissipation	T_A=25℃	P_D	2.1	W
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient *Note2		$R_{\theta JA}$	60	℃/W

Notes:

1. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
2. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design. $R_{\theta JA}$ shown below for single device operation on FR-4 in still air.

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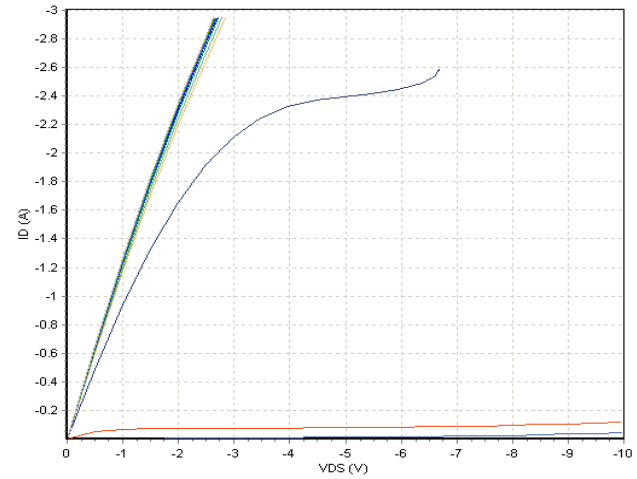
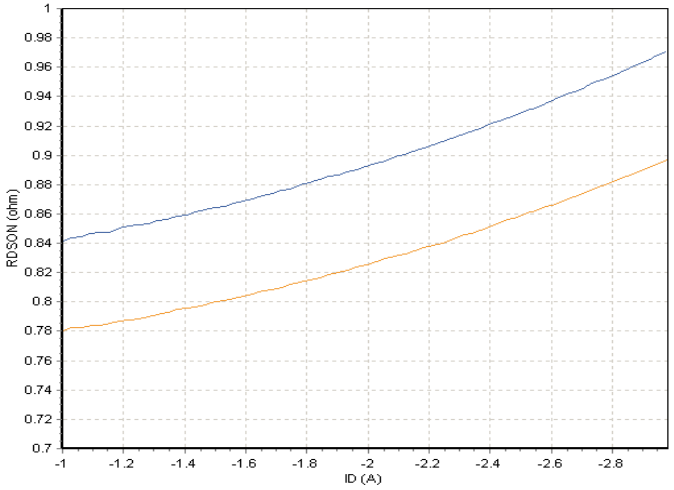
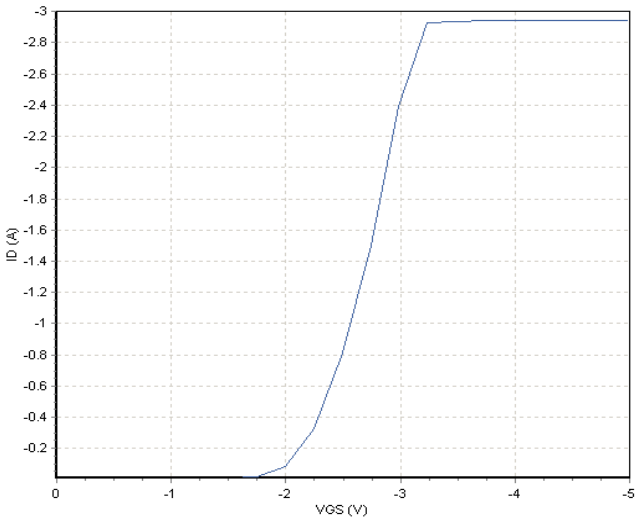
ELECTRICAL CHARACTERISTICS (T_A=25℃ Unless otherwise noted)

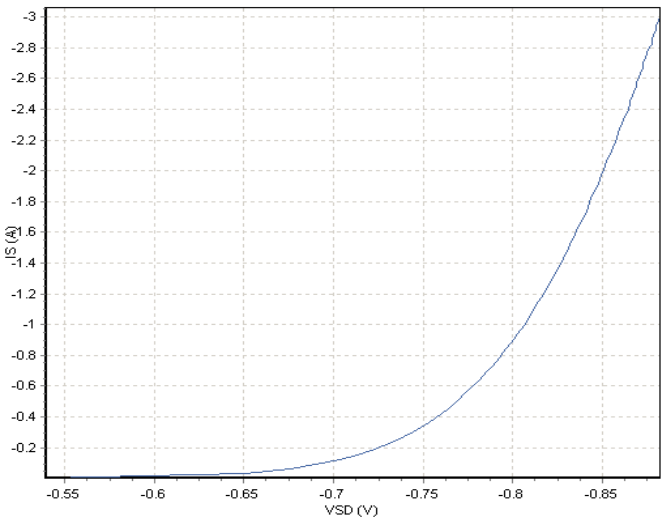
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-150			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250uA	-1		-3.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-120V,V_{GS}=0V, T_J=25℃			-1	uA
On-State Drain Current	$I_{D(on)}$	V_{DS}=V_{GS} =0V			-1.0	A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-1A		780	900	mΩ
		V_{GS}=-4.5V,I_D=-1A		880	1000	mΩ
Forward Transconductance	gfs	V_{DS}=-10V,I_D=-1A		2.4		S
Diode Forward Voltage	V_{SD}	I_S=-1A,V_{GS} =0V	-0.4		-1.0	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=-75V,V_{GS}=-10V I_D=-1A		20		nC
Gate-Source Charge	Q_{gs}			5		
Gate-Drain Charge	Q_{gd}			8		
Input Capacitance	C_{iss}	V_{DS}=-75,V_{GS}=0V f=1MHz		750		pF
Output Capacitance	C_{oss}			48		
Reverse Transfer Capacitance	C_{rss}			20		
Turn-On Time	$t_{d(on)}$	V_{DD}=-75V , V_{GS}=-10V, R_G=3.0Ω		12		nS
	t_r			32		
Turn-Off Time	$t_{d(off)}$			30		
	t_f			10		

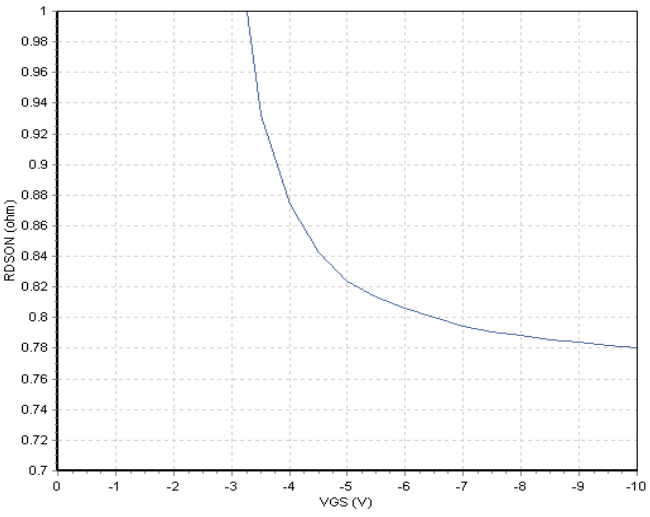
TYPICAL CHARACTERISTIC











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