



SPP2327

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP2327 is the P-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. The SPP2327 has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

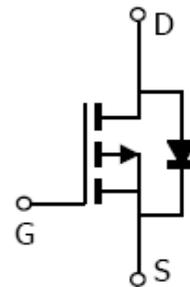
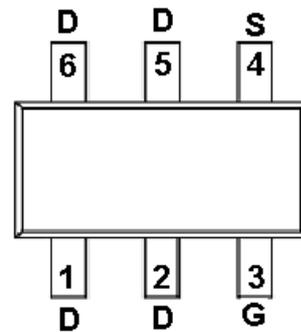
APPLICATIONS

- Powered System
- DC/DC Converter
- Load Switch

FEATURES

- ◆ $-100V/-0.8A$, $R_{DS(ON)}=650m\Omega@V_{GS}=-10V$
- ◆ $-100V/-0.4A$, $R_{DS(ON)}=750m\Omega@V_{GS}=-4.5V$
- ◆ High density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-23-6L package design

PIN CONFIGURATION(SOT-23-6L)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	D	Drain
2	D	Drain
3	G	Gate
4	S	Source
5	D	Drain
6	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP2327S26RGB	SOT-23-6L	27YW

※ SPP2327S26RGB : Tape Reel ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS (TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit	
Drain-Source Voltage	V _{DSS}	-100	V	
Gate –Source Voltage	V _{GSS}	±20	V	
Continuous Drain Current	I _D	TA=25°C	-1.5	A
		TA=70°C	-1.2	
Pulsed Drain Current	I _{DM}	-4.5	A	
Power Dissipation	P _D	TA=25°C	1.15	W
		TA=70°C	0.8	
Operating Junction Temperature	T _J	-55/150	°C	
Storage Temperature Range	T _{STG}	-55/150	°C	
Thermal Resistance-Junction to Ambient	R _{θJA}	100	°C/W	



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ELECTRICAL CHARACTERISTICS (T_A=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =-250uA	-100			V	
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-1	-1.5	-2.5		
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-80V, V _{GS} =0V, T _J =25°C			1	uA	
		V _{DS} =-80V, V _{GS} =0V T _J =55°C			10		
On-State Drain Current	I _{D(on)}	V _{DS} =V _{GS} =0V	-		-1.5	A	
Drain-Source On-Resistance	R _{DSS(on)}	V _{GS} =-10V, I _D =-0.8A		0.52	0.65	Ω	
		V _{GS} =-4.5V, I _D =-0.4A		0.6	0.75	Ω	
Forward Transconductance	g _{fs}	V _{DS} =-10V, I _D =-1A		2.9		S	
Diode Forward Voltage	V _{SD}	I _S =-0.5A, V _{GS} =0V			-1.2	V	
Dynamic							
Total Gate Charge	Q _g	V _{DS} =-50V, V _{GS} =-10V I _D =-1A		9.3		nC	
Gate-Source Charge	Q _{gs}			1.75			
Gate-Drain Charge	Q _{gd}			1.25			
Input Capacitance	C _{iss}	V _{DS} =-15, V _{GS} =0V f=1MHz		553		pF	
Output Capacitance	C _{oss}			29			
Reverse Transfer Capacitance	C _{rss}			20			
Turn-On Time	t _{d(on)}	V _{DD} =-50V, I _D =-0.5A, V _{GS} =-10V, R _G =3.3Ω		2		nS	
	t _r			18.4			
Turn-Off Time	t _{d(off)}				19.6		
	t _f				19.5		



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TYPICAL CHARACTERISTICS

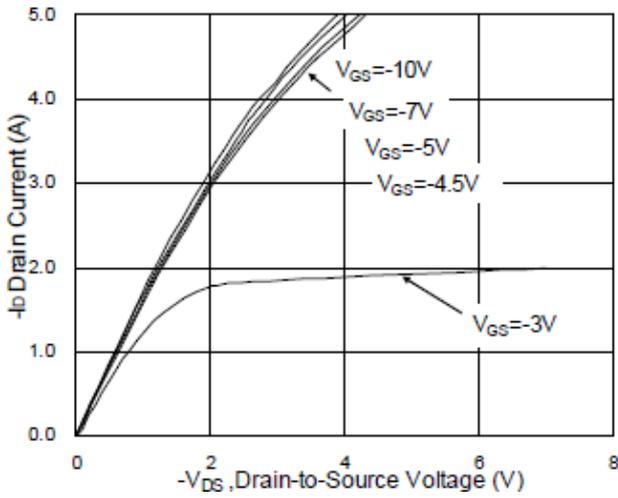


Fig 1 Output Characteristics

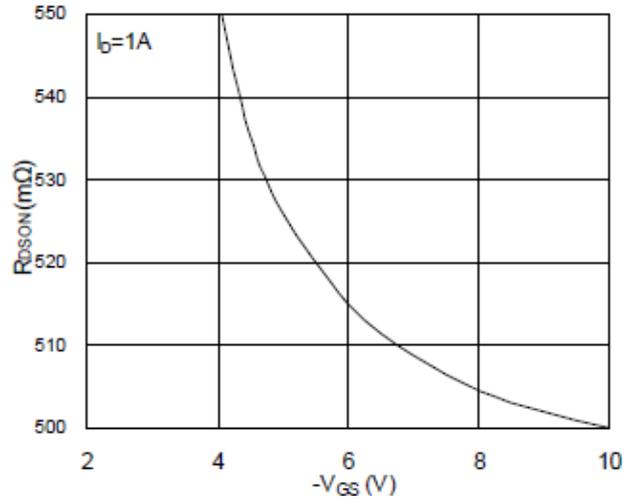


Fig. 2 On-Resistance vs Gate Source Voltage

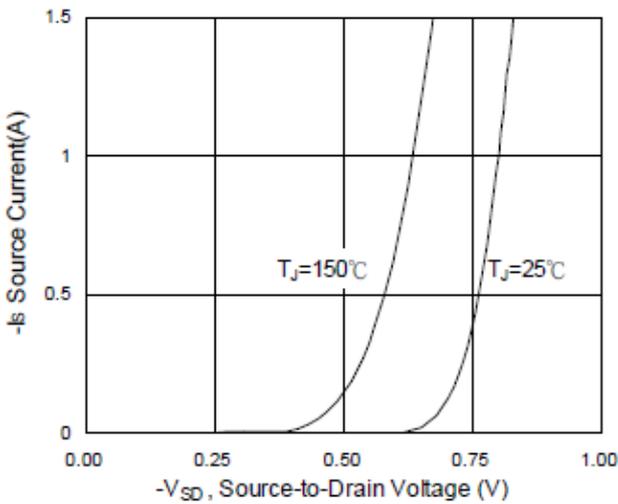


Fig 3 Source-Drain Forward Voltage

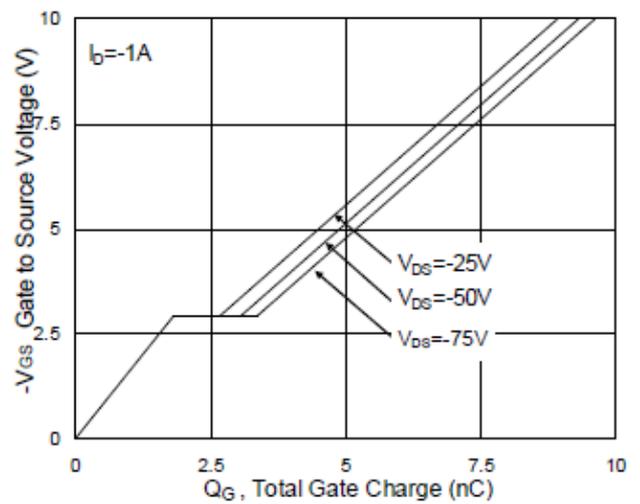


Fig. 4 Gate Charge

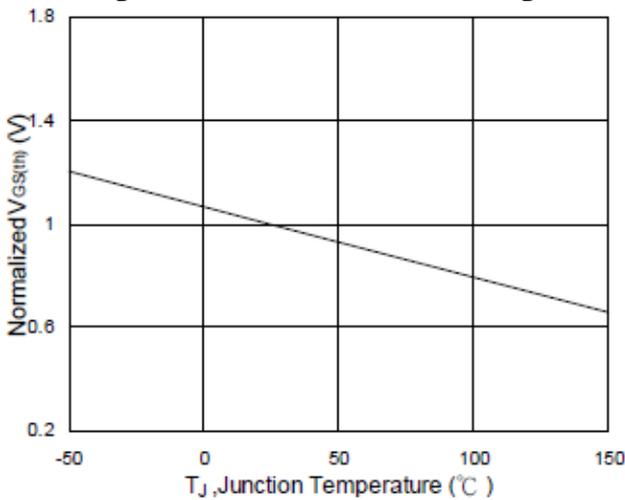


Fig. 5 Gate Voltage vs Junction temperature

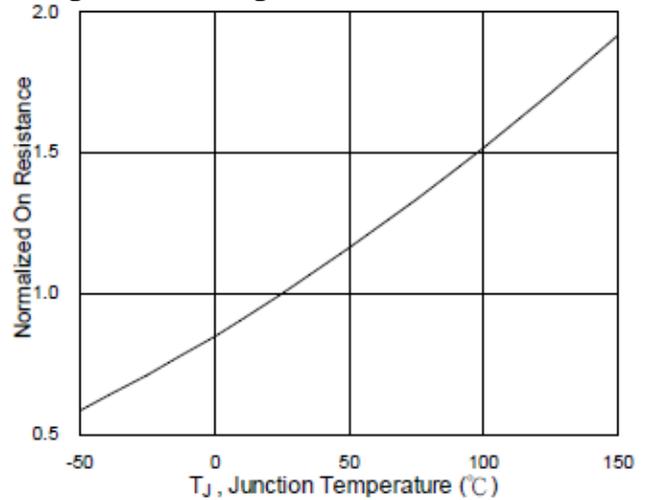


Fig. 6 On-Resistance vs Junction Temperature



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TYPICAL CHARACTERISTICS

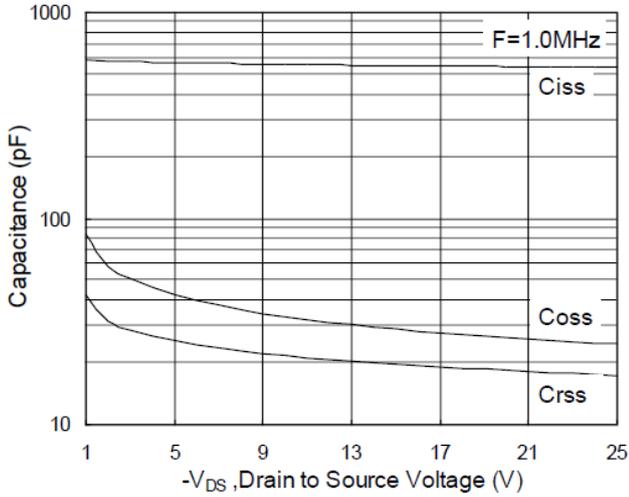


Fig. 7 Capacitance vs Vds

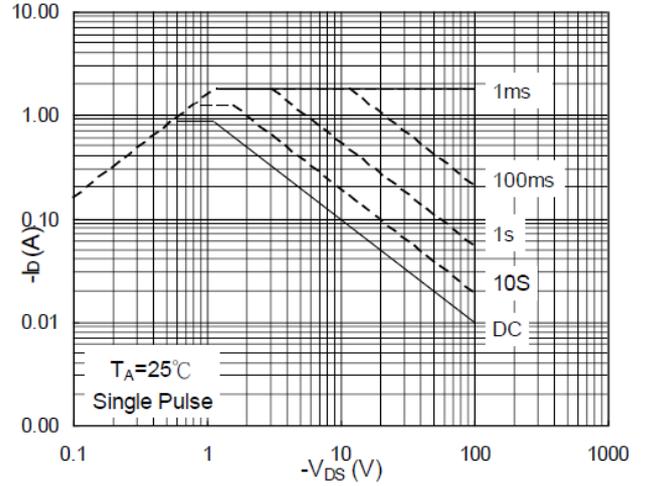


Fig. 8 Safe Operation Area

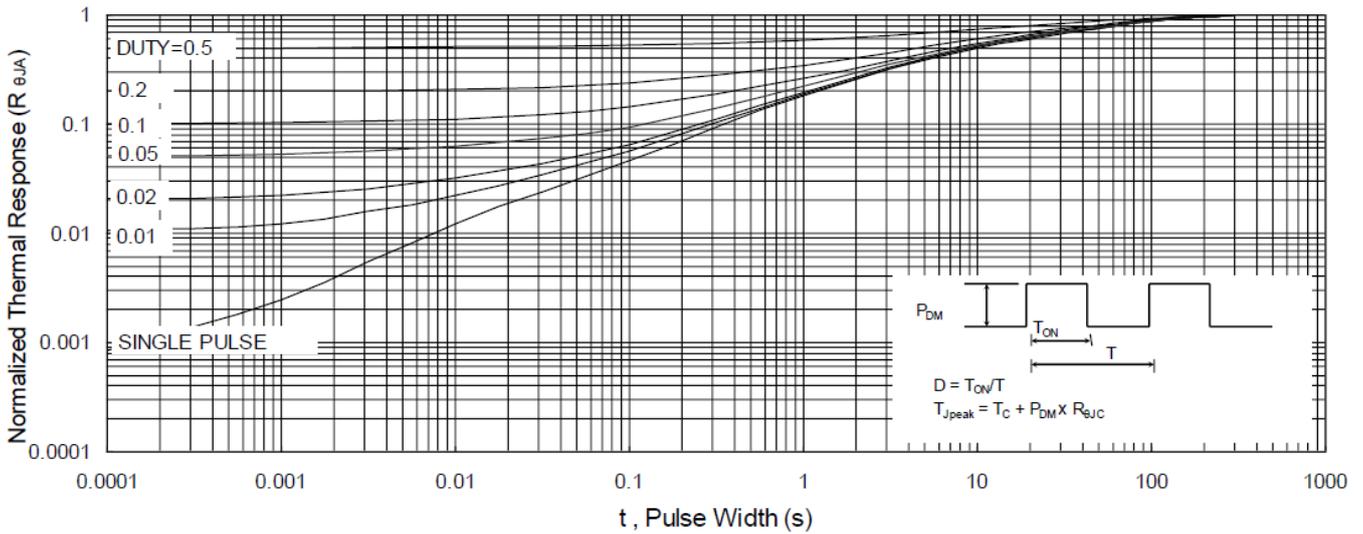


Fig. 9 Normalized Maximum Transient Thermal Resistance



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