



SPN8846

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN8846 is the N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

FEATURES

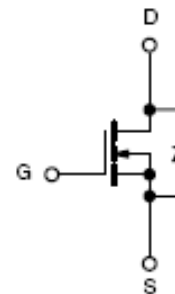
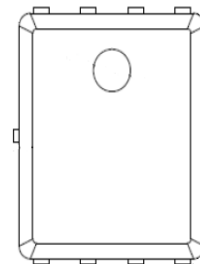
- ◆ 40V/125A, $R_{DS(ON)}=3.8m\Omega@V_{GS}=10V$
- ◆ 40V/125A, $R_{DS(ON)}=5.3m\Omega@V_{GS}=4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ PPAK5x6-8L package design

APPLICATIONS

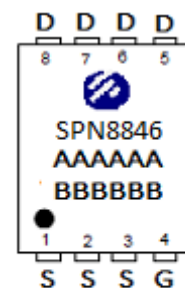
- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier
- Motor Control
- Power Tool

PIN CONFIGURATION

PPAK5x6-8L



PART MARKING



A : Lot Code
B : Date Code
(YY/MM/DD)



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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8846DN8RGB	PPAK5x6-8L	SPN8846

※ SPN8846DN8RGB : Tape&Reel ; Pb – Free ; Halogen - Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	40	V
Gate –Source Voltage		V _{GSS}	±20	V
Continuous Drain Current(Silicon Limited)	T _C =25°C	I _D	101	A
	T _C =100°C		64	
Pulsed Drain Current		I _{DM}	220	A
Power Dissipation @ T _C =25°C		P _D	83	W
Avalanche Energy with Single Pulse (T _C =25°C, L = 0.1mH.)		E _{AS}	145	mJ
Operating Junction Temperature		T _J	-55~150	°C
Storage Temperature Range		T _{STG}	-55~150	°C
Thermal Resistance-Junction to Case		R _{θJC}	1.5	°C/W

Note :

The maximum current rating is package limited at 80A for PPAK5x6-8L



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ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =250uA	40			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250uA	1	1.8	2.2	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V T _J = 25 °C			1	uA
		V _{DS} =40V, V _{GS} =0V T _J = 125 °C			100	
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =20A			3.8	mΩ
		V _{GS} =4.5V, I _D =20A			5.3	
Forward Transconductance	g _{fs}	V _{DS} =5V, I _D =20A		75		S
Gate Resistance	R _G	V _{GS} =0V, V _{DS} =Open, f=1MHz		1.5		Ω
Diode Forward Voltage	V _{SD}	I _F =1A, V _{GS} =0V			1	V
Dynamic						
Total Gate Charge (10V)	Q _g	V _{DS} =20V, V _{GS} =10V I _D =20A		44		nC
Total Gate Charge (4.5V)	Q _g			23		
Gate-Source Charge	Q _{gs}			7.5		
Gate-Drain Charge	Q _{gd}			5.5		
Input Capacitance	C _{iss}	V _{DS} =20V, V _{GS} =0V f=1MHz		2648		pF
Output Capacitance	C _{oss}			899		
Reverse Transfer Capacitance	C _{rss}			71		
Turn-On Time	td(on)	V _{DD} =20V, I _D =20A V _{GEN} =10V, R _G =3Ω		10		nS
	tr			5		
Turn-Off Time	td(off)			33		
	tf			6.5		



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TYPICAL CHARACTERISTICS

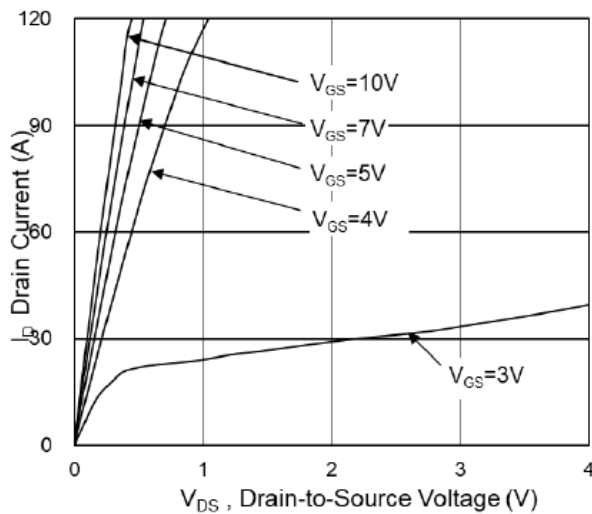


Fig. 1 Typical Output Characteristics

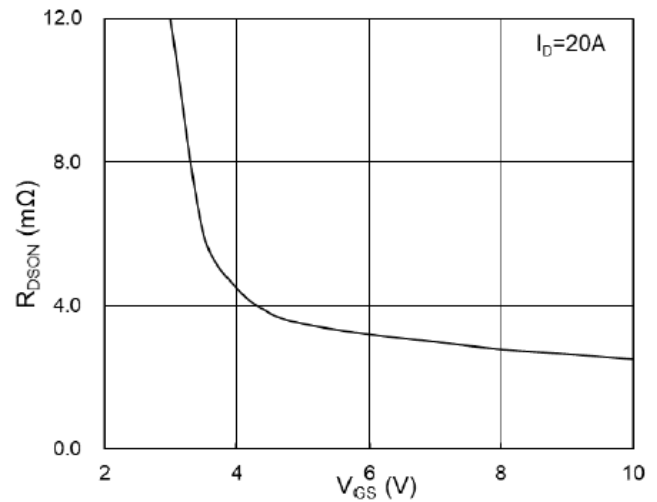


Fig. 2 On-Resistance vs. V_{GS}

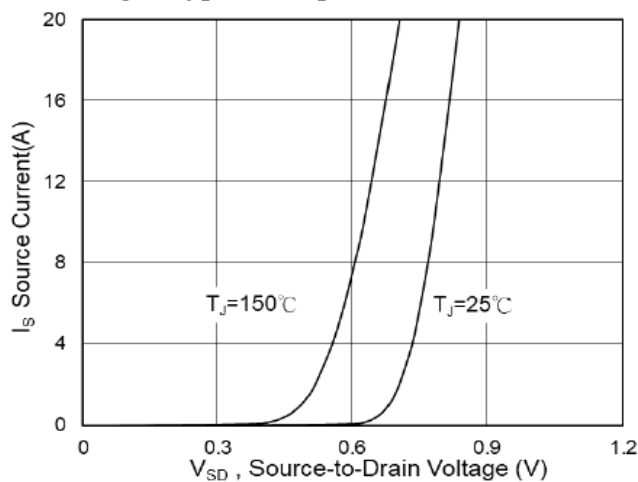


Fig. 3 Source-Drain Forward Characteristics

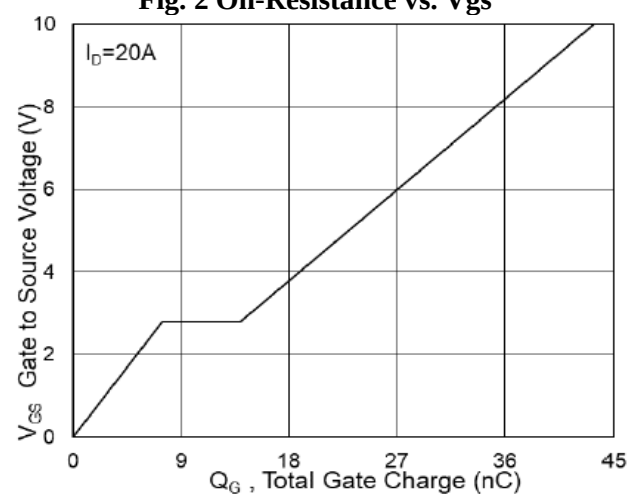


Fig. 4 Gate Charge Characteristics

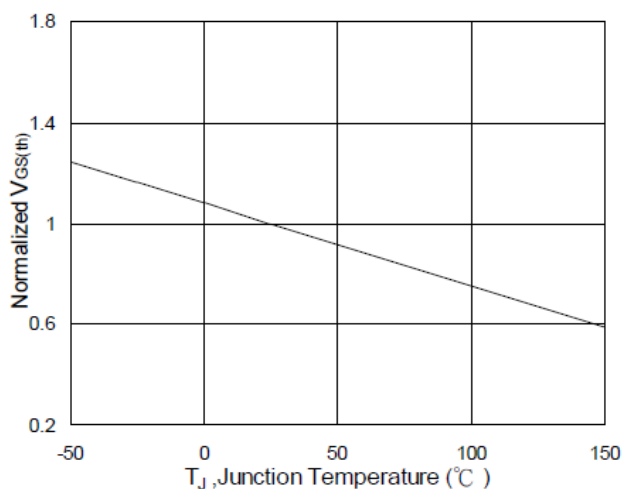


Fig. 5 Normalized V_{GS} vs T_J

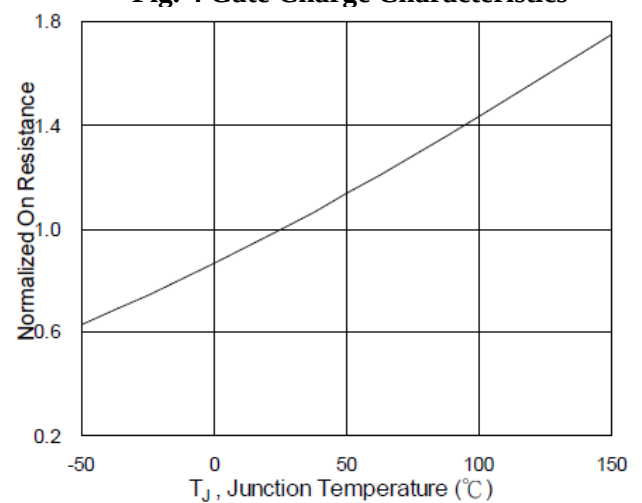


Fig. 6 Normalized $R_{DS(on)}$ vs T_J



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TYPICAL CHARACTERISTICS

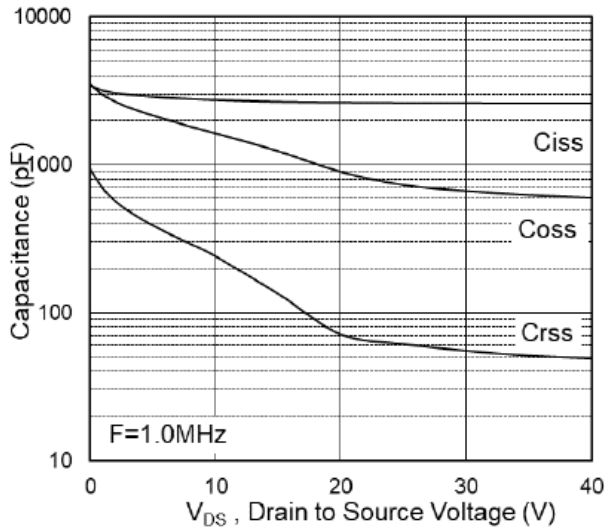


Fig. 7 Capacitance

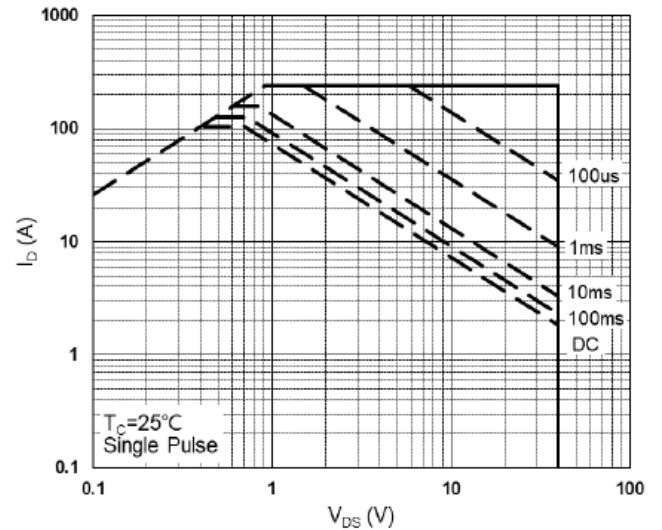


Fig. 8 Safe Operation Area

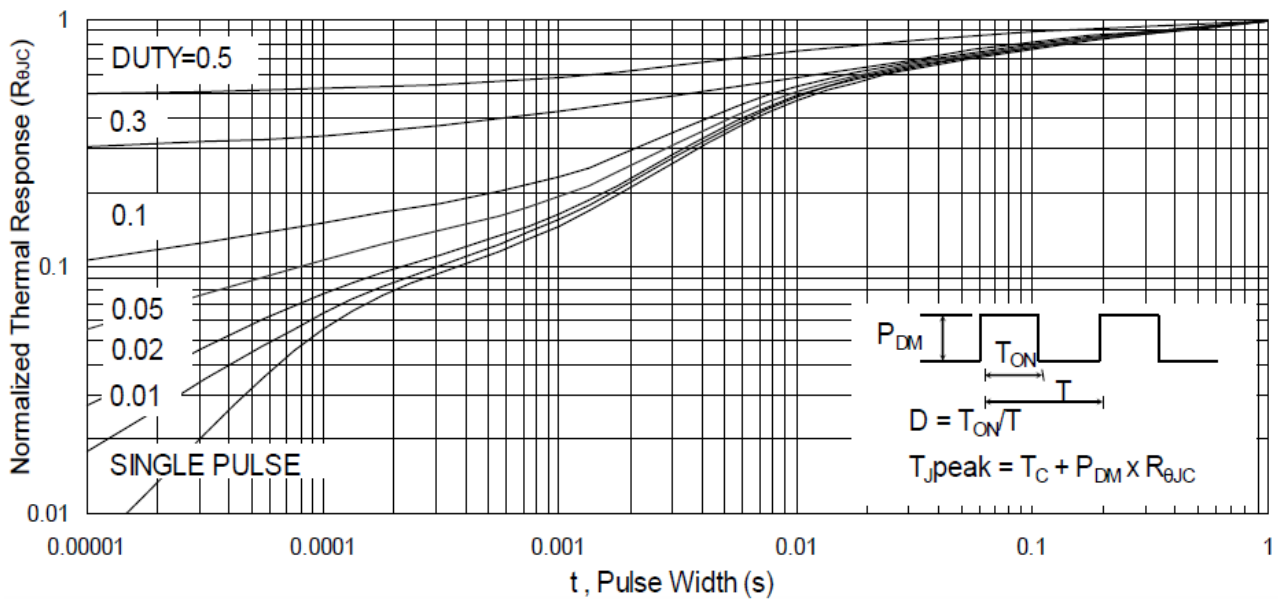


Fig. 9 Normalized Maximum Transient Thermal Impedance



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Date	ver.	Description
2024/01/12	0.1	Preliminary 版發行
2024/01/18	0.2	Remove Maximum Current for TO220/TO252 package
2024/02/19	0.3	Modify parameter item :I _{DSS} @V _{DS} voltage from 45V to 40V by Michael