SPN8846
N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN8846 is the N-Channel logic enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

APPLICATIONS

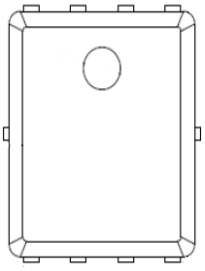
- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier
- Motor Control
- Power Tool

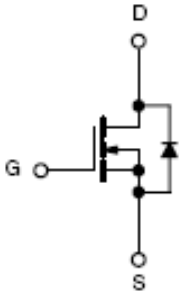
FEATURES

- 40V/125A, $R_{DS(ON)}$=3.8mΩ@V_{GS}=10V
- 40V/125A, $R_{DS(ON)}$=5.3mΩ@V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- PPAK5x6-8L package design

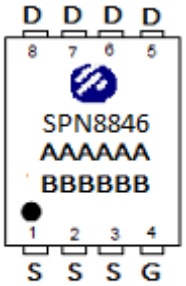
PIN CONFIGURATION

PPAK5x6-8L





PART MARKING



A : Lot Code
B : Date Code
(YY / MM / DD)

SPN8846
N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN8846DN8RGB	PPAK5x6-8L	SPN8846

※ SPN8846DN8RGB : Tape&Reel ; Pb – Free ; Halogen - Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	40	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(Silicon Limited)	T_C=25℃	I_D	101	A
	T_C=100℃		64	
Pulsed Drain Current		I_{DM}	220	A
Power Dissipation @ T_C=25℃		P_D	83	W
Avalanche Energy with Single Pulse (T_C=25℃, L = 0.1mH.)		E_{AS}	145	mJ
Operating Junction Temperature		T_J	-55~150	℃
Storage Temperature Range		T_{STG}	-55~150	℃
Thermal Resistance-Junction to Case		$R_{\theta JC}$	1.5	℃/W

Note :
The maximum current rating is package limited at 80A for PPAK5x6-8L

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	40			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	1	1.8	2.2	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V, V_{GS}=0V T_J = 25 ℃			1	uA
		V_{DS}=40V, V_{GS}=0V T_J = 125 ℃			100	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=20A			3.8	mΩ
		V_{GS}=4.5V,I_D=20A			5.3	
Forward Transconductance	gfs	V_{DS}=5V,I_D=20A		75		S
Gate Resistance	R_G	V_{GS}=0V,V_{DS}=Open, f=1MHz		1.5		Ω
Diode Forward Voltage	V_{SD}	I_F=1A ,V_{GS} =0V			1	V
Dynamic						
Total Gate Charge (10V)	Q_g	V_{DS}=20V, V_{GS}=10V I_D=20A		44		nC
Total Gate Charge (4.5V)	Q_g			23		
Gate-Source Charge	Q_{gs}			7.5		
Gate-Drain Charge	Q_{gd}			5.5		
Input Capacitance	C_{iss}	V_{DS}=20V, V_{GS}=0V f=1MHz		2648		pF
Output Capacitance	C_{oss}			899		
Reverse Transfer Capacitance	C_{rss}			71		
Turn-On Time	td(on)	V_{DD}=20V, ID=20A V_{GEN}=10V, R_G=3Ω		10		nS
	tr			5		
Turn-Off Time	td(off)			33		
	tf			6.5		

TYPICAL CHARACTERISTICS

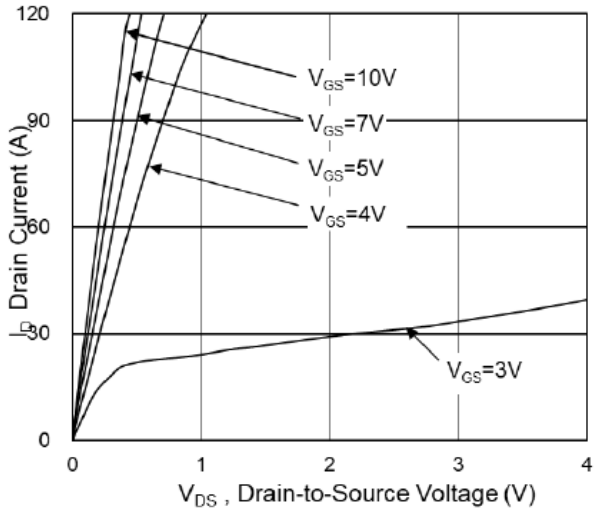


Fig. 1 Typical Output Characteristics

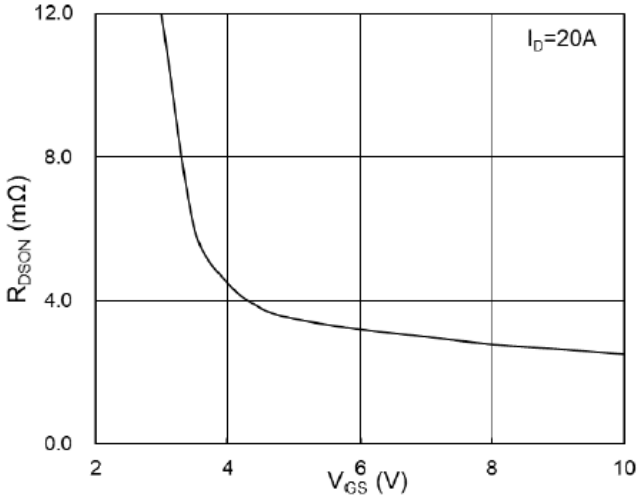


Fig. 2 On-Resistance vs. Vgs

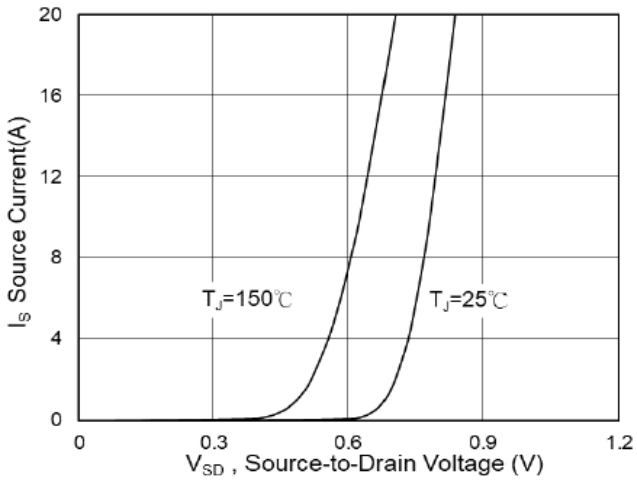


Fig. 3 Source-Drain Forward Characteristics

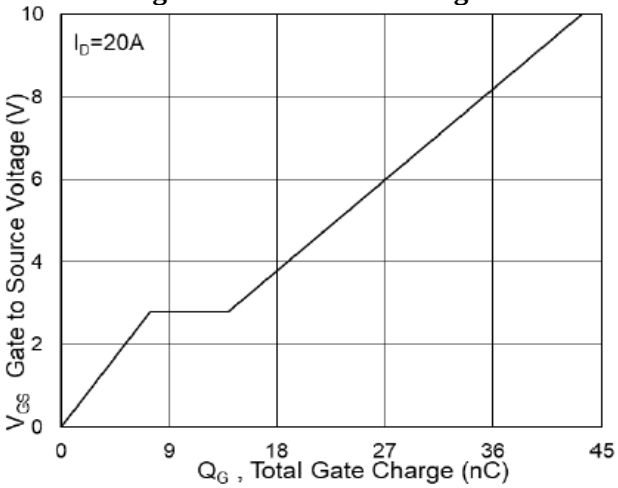


Fig. 4 Gate Charge Characteristics

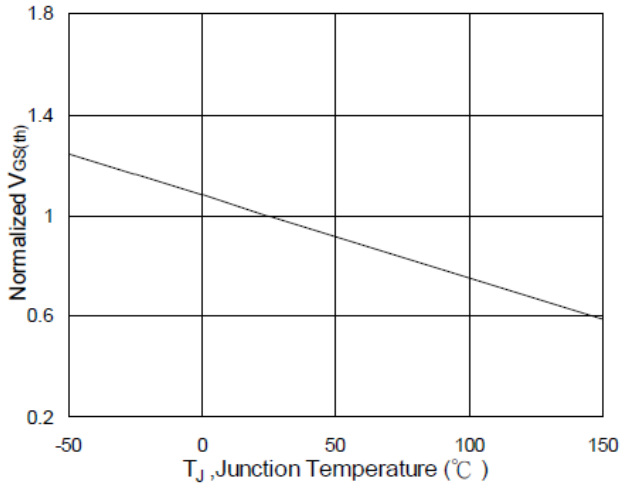


Fig. 5 Normalized Vgs vs Tj

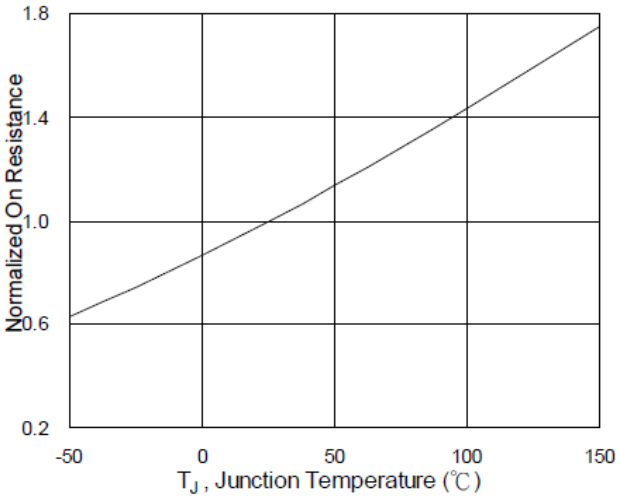


Fig. 6 Normalized Rdson vs Tj

TYPICAL CHARACTERISTICS

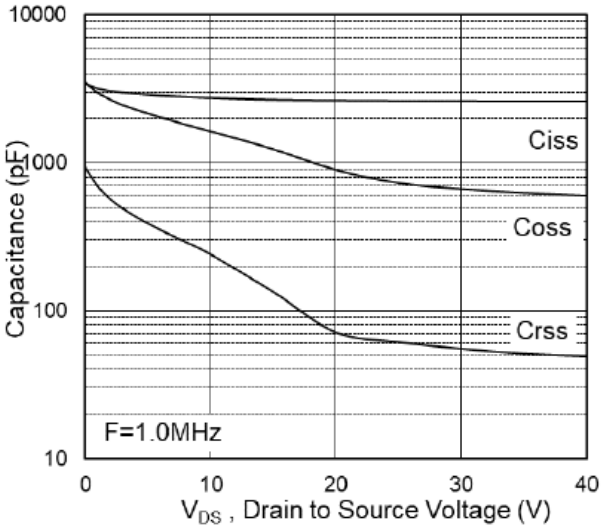


Fig. 7 Capacitance

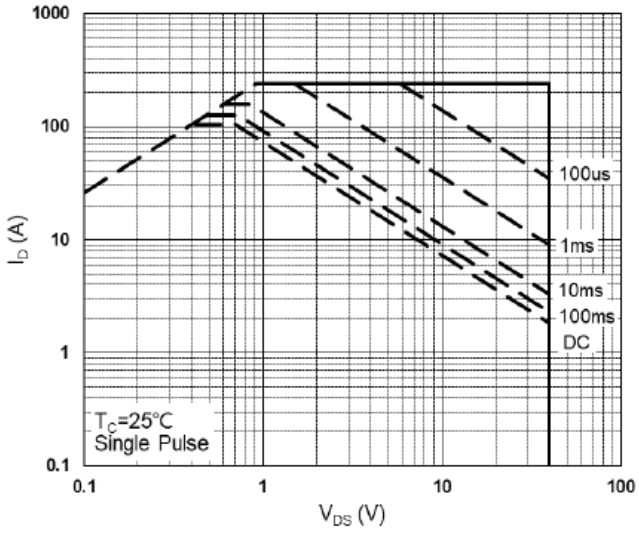


Fig. 8 Safe Operation Area

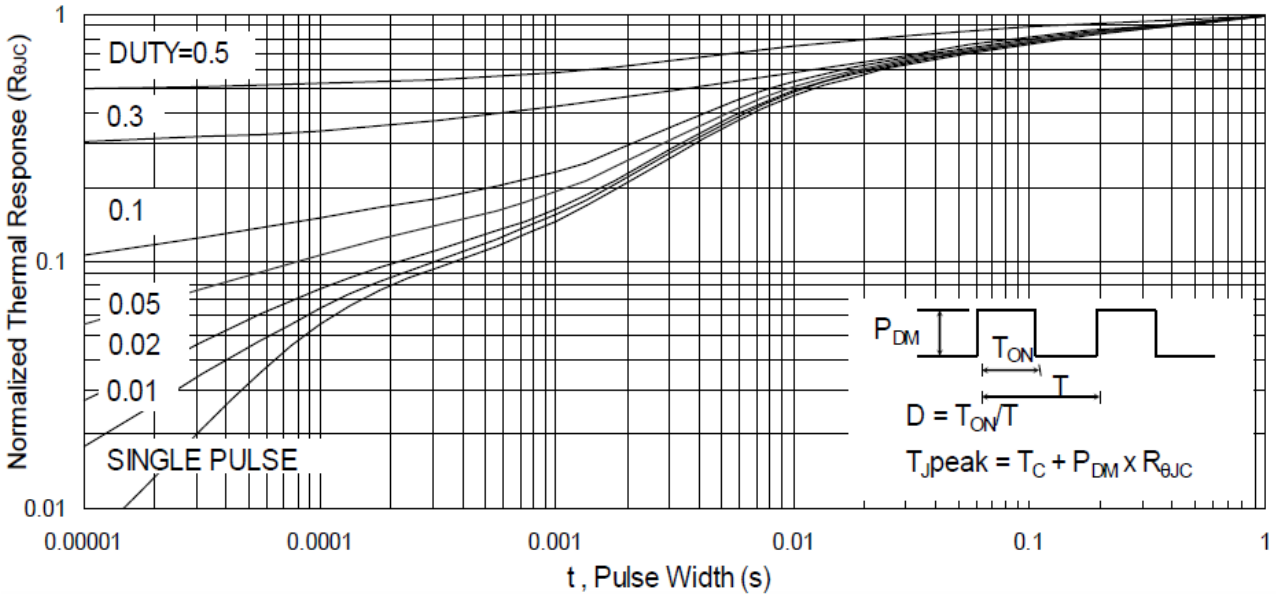


Fig. 9 Normalized Maximum Transient Thermal Impedance

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Date	ver.	Description
2024/01/12	0.1	Preliminary 版發行
2024/01/18	0.2	Remove Maximum Current for TO220/TO252 package
2024/02/19	0.3	Modify parameter item :I_{DSS} @V_{DS} voltage from 45V to 40V by Michael