



# SPN5001

## N-Channel Enhancement Mode MOSFET

### DESCRIPTION

The SPN5001 is the N-Channel enhancement mode power field effect transistor which is produced with high voltage BiCMOS technology. This device is particularly suited for reducing the no load consumption in PC power, TV power and Adapter.

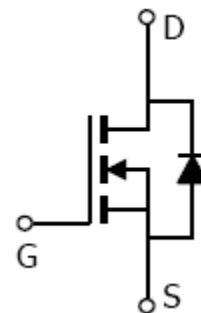
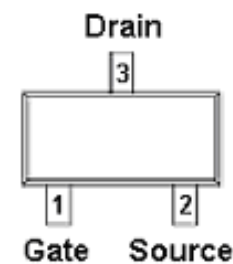
### APPLICATIONS

- Desk PC Power Supply
- AC adapter
- LCD TC Power Supply

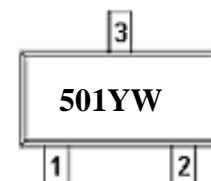
### FEATURES

- ◆ 600V/27mA ,  $R_{DS(ON)}=300\Omega @ V_{GS}=10V$
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOT-23 package design

### PIN CONFIGURATION(SOT-23)



### PART MARKING



YW: Date Code



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### PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPN5001S23RGB	SOT-23	501

※ SPN5001S23RGB : Tape Reel ; Pb – Free ; Halogen – Free

### ABSOLUTE MAXIMUM RATINGS (TA=25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V <sub>DSS</sub>	600	V
Gate –Source Voltage - Continuous		V <sub>GSS</sub>	±20	V
Continuous Drain Current	TA=25°C	I <sub>D</sub>	27	mA
Power Dissipation	TA=25°C	P <sub>D</sub>	0.5	W
Operating Junction Temperature		T <sub>J</sub>	-55 ~ 150	°C
Storage Temperature Range		T <sub>STG</sub>	-55 ~ 150	°C
Thermal Resistance-Junction to Ambient		R <sub>θJA</sub>	250	°C/W



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### ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	600			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	3.0		4.5	
Gate Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =480V, V <sub>GS</sub> =0V T <sub>J</sub> =25°C			25	uA
Drain-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =16mA			300	Ω
Forward Transconductance	G <sub>fs(1)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> =16mA		28		mS
<b>Dynamic</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DD</sub> = 200 V, I <sub>D</sub> = 0.1 A, V <sub>GS</sub> = 10 V	1.8	2.5	3.2	nC
Gate-Source Charge	Q <sub>gs</sub>			1.3		
Gate-Drain Charge	Q <sub>gd</sub>			0.8		
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 25 V, f = 1 MHz, V <sub>GS</sub> = 0	8.8	12.5	16.2	pF
Output Capacitance	C <sub>oss</sub>		7	10	13	
Reverse Transfer Capacitance	C <sub>rss</sub>		5	7	9	
Turn-On Time	t <sub>d(on)</sub>	V <sub>DS</sub> = 300 V, I <sub>D</sub> = 10m A R <sub>G</sub> = 3.3Ω V <sub>GS</sub> = 10.0 V R <sub>D</sub> = 30kΩ		11.5		nS
	t <sub>r</sub>			14.5		
Turn-Off Time	t <sub>d(off)</sub>			14		
	t <sub>f</sub>			120		



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### TYPICAL CHARACTERISTICS

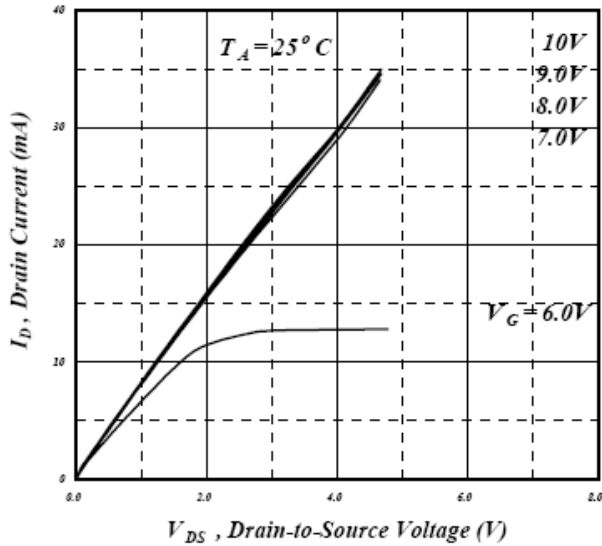


Fig 1. Typical Output Characteristics

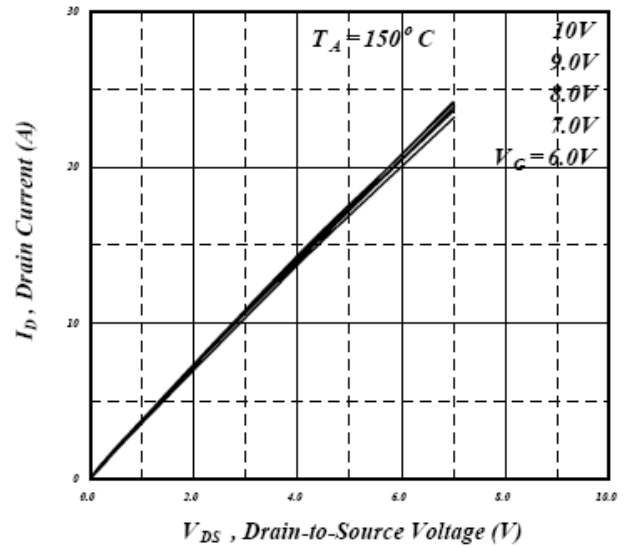


Fig 2. Typical Output Characteristics

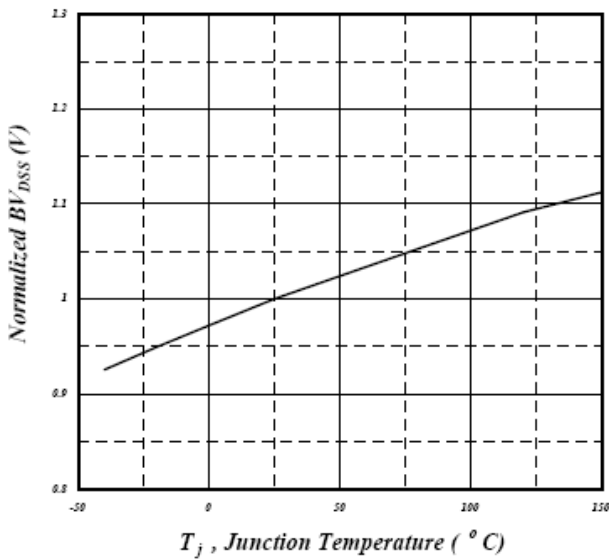


Fig 3. Normalized  $BV_{DSS}$  v.s. Junction Temperature

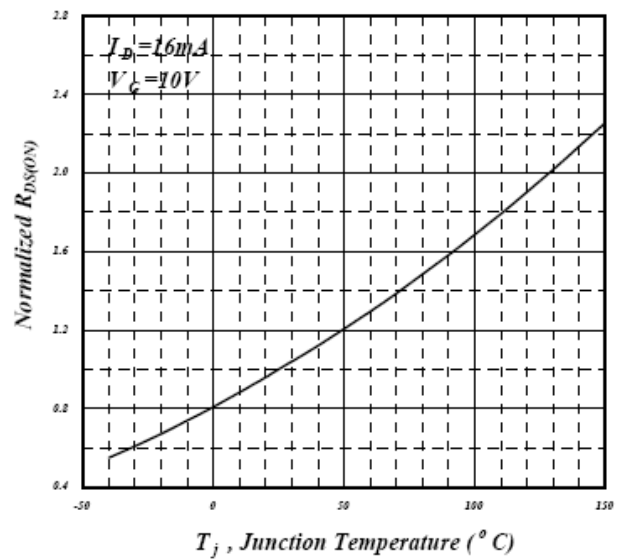


Fig 4. Normalized On-Resistance v.s. Junction Temperature



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### TYPICAL CHARACTERISTICS

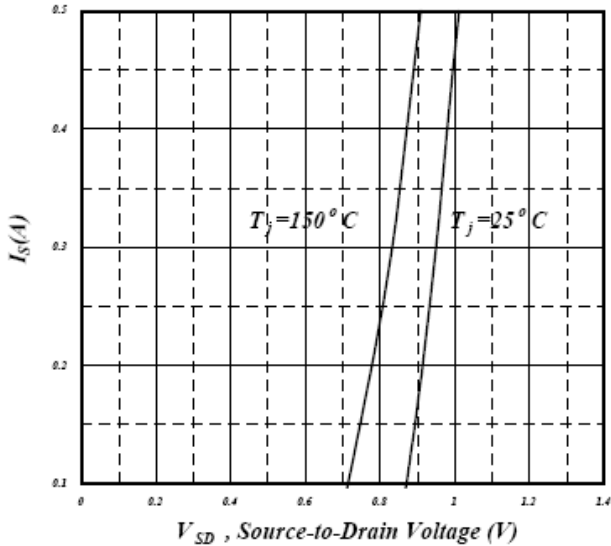


Fig 5. Forward Characteristic of Reverse Diode

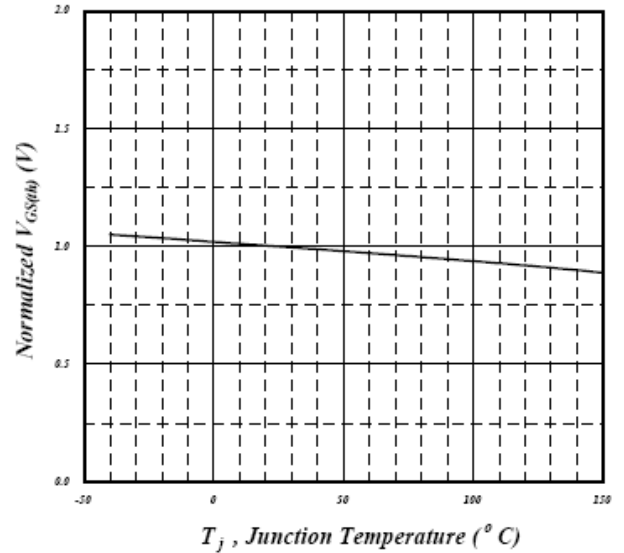


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

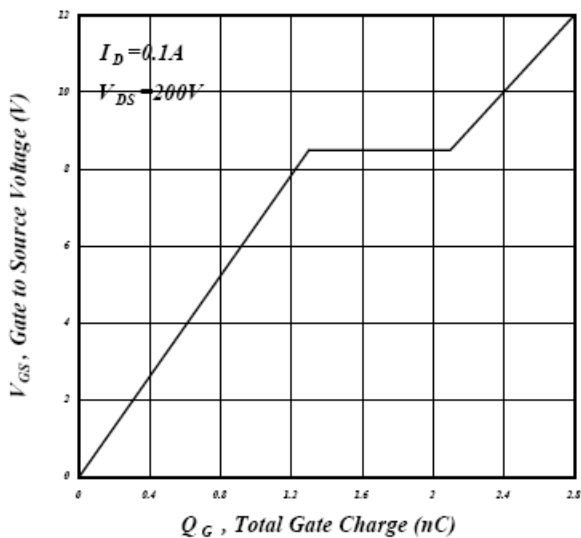


Fig 7. Gate Charge Characteristics

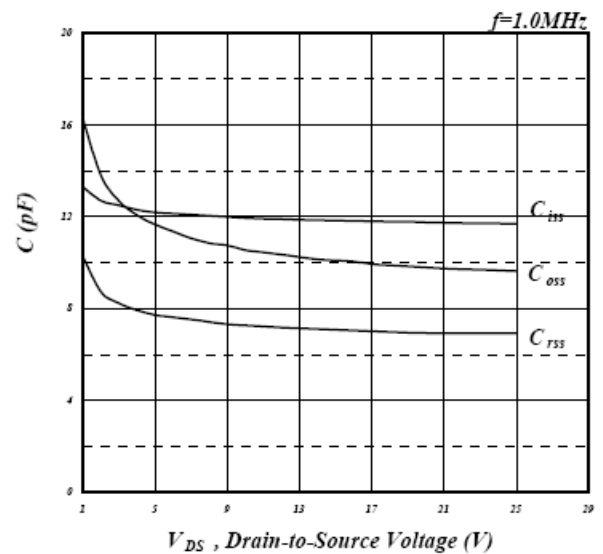


Fig 8. Typical Capacitance Characteristics



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### TYPICAL CHARACTERISTICS

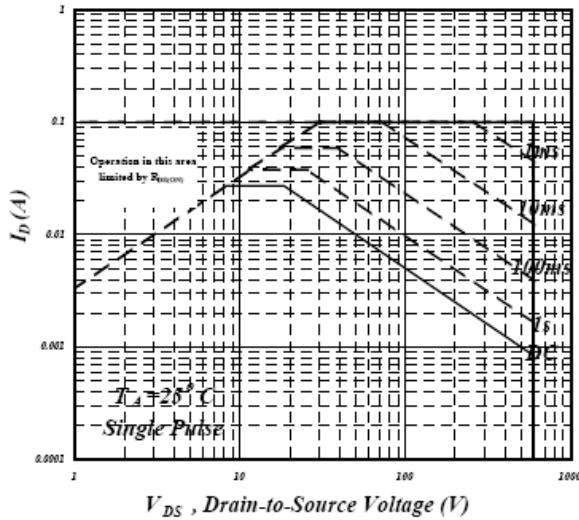


Fig 9. Maximum Safe Operating Area

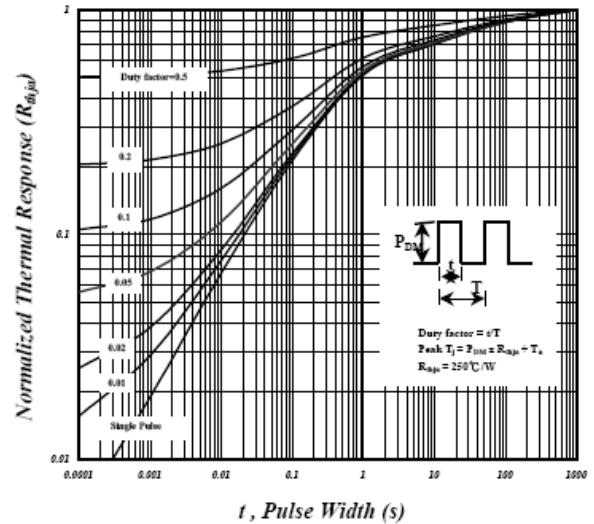


Fig 10. Effective Transient Thermal Impedance

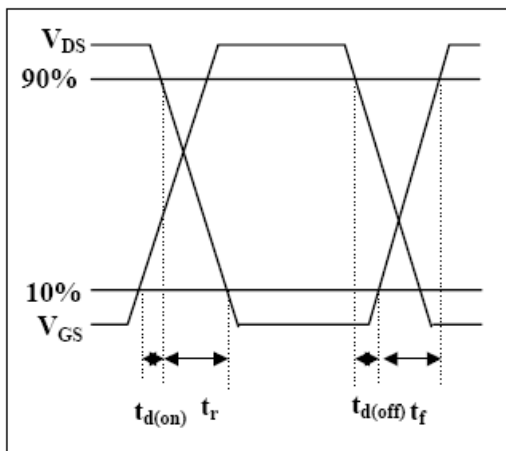


Fig 11. Switching Time Waveform

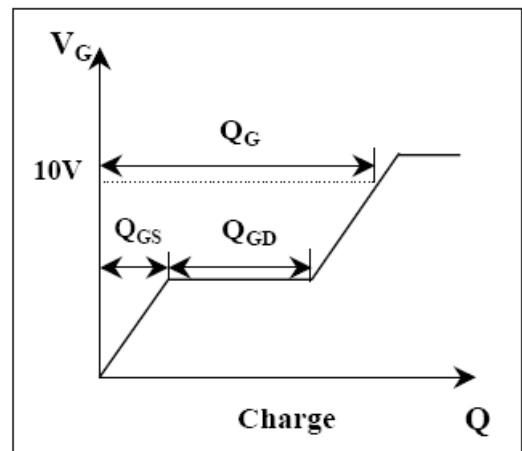


Fig 12. Gate Charge Circuit



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