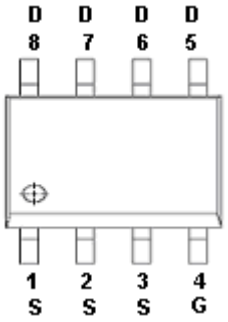
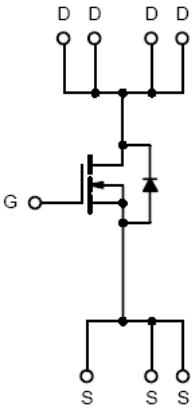
SPN4866
N-Channel Enhancement Mode MOSFET

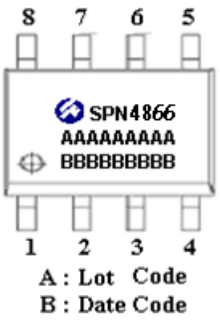
DESCRIPTION
The SPN4866 is the N-Channel enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.
This high density process is especially tailored to minimize on-state resistance.
These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high efficiency and fast switching is required.

APPLICATIONS
- Motor Drive
- Power Tools
- LED Lighting
- Quick Charger

FEATURES
- 60V/6A,$R_{DS(ON)}$=16mΩ@V_{GS}=10V
- 60V/6A,$R_{DS(ON)}$=20mΩ@V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOP-8 package design

PIN CONFIGURATION (SOP–8)




PART MARKING


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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN4866S8RGB	SOP-8	SPN4866

※ SPN4866S8RGB : Tape Reel ; Pb – Free; Halogen - Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	60	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150℃)	T_C=25℃	I_D	6.5	A
	T_C=100℃		4.1	
Pulsed Drain Current		I_{DM}	26	A
Avalanche Energy Single Pulse(L=0.1mH, T_C=25℃)		E_{AS}	36	mJ
Power Dissipation	T_A=25℃	P_D	1.5	W
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	85	℃/W
Thermal Resistance-Junction to Case		$R_{\theta JC}$	23	℃/W

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ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250uA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_{DS}=250uA	1.3		3.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=48V,V_{GS}=0V, T_J=25℃			1	uA
		V_{DS}=48V,V_{GS}=0V, T_J=150℃			100	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=6A		13	16	mΩ
		V_{GS}=4.5V,I_D=6A		16	20	
Gate Resistance	R_G			1.3		Ω
Forward Transconductance	gfs	V_{DS}=10V, I_D=3A		15		S
Diode Forward Voltage	V_{SD}	I_S=6A,V_{GS}=0V			1.2	V
Dynamic						
Total Gate Charge	$Q_{g(10V)}$	V_{DS}=48V,V_{GS}=10V, I_D=6A		29		nC
Gate-Source Charge	Q_{gs}			4		
Gate-Drain Charge	Q_{gd}			8		
Total Gate Charge	$Q_{g(4.5V)}$	V_{DS}=48V,V_{GS}=4.5V I_D=6A		15		
Input Capacitance	C_{iss}	V_{GS}=0V,V_{DS}=25V, F=1MHz		1400		pF
Output Capacitance	C_{oss}			137		
Reverse Transfer Capacitance	C_{rss}			95		
Turn-On Time	$t_{d(on)}$	(V_{DD}=48V,I_D=6A, V_{GEN}=10V,R_G=2.5Ω)		8.4		nS
	t_r			12.4		
Turn-Off Time	$t_{d(off)}$			26		
	t_f			4.4		

TYPICAL CHARACTERISTICS

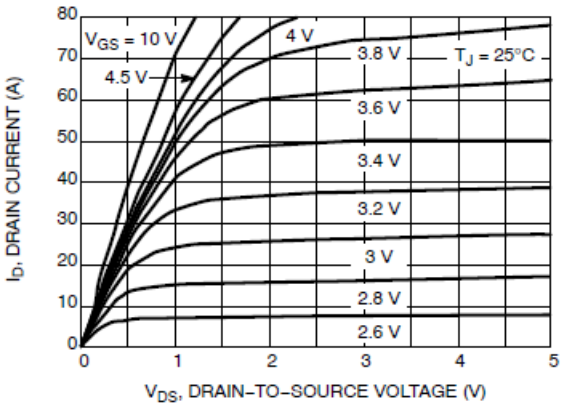

Figure 1. On−Region Characteristics

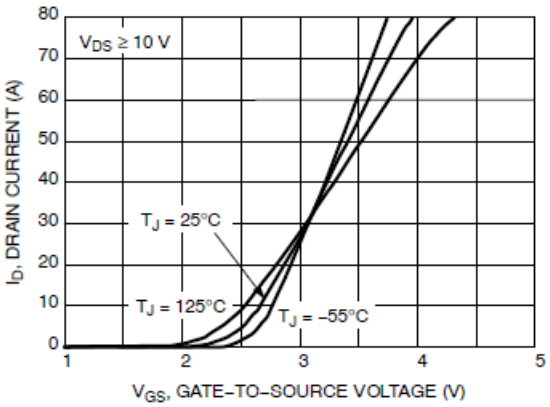

Figure 2. Transfer Characteristics

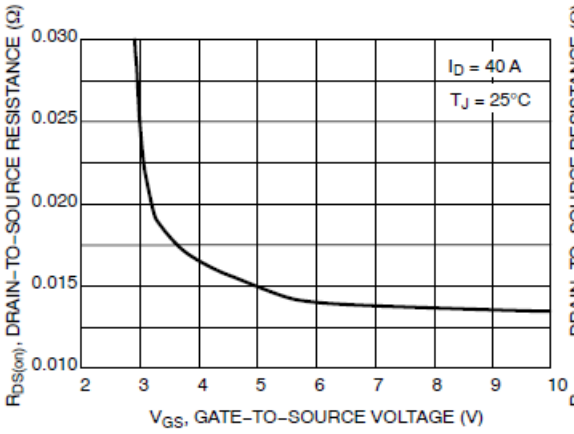

Figure 3. On−Resistance vs. Gate Voltage

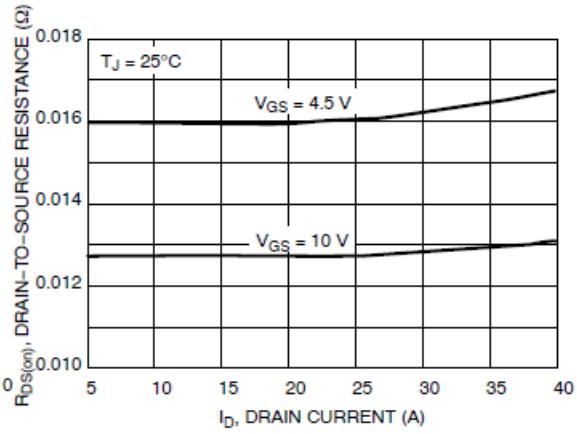

Figure 4. On−Resistance vs. Drain Current

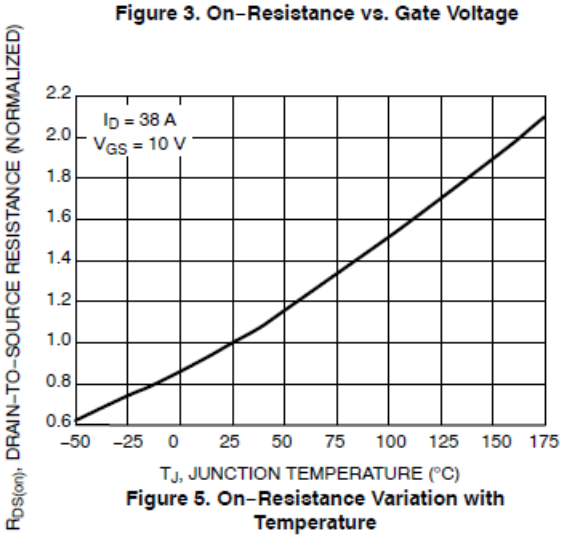

Figure 5. On−Resistance Variation with Temperature

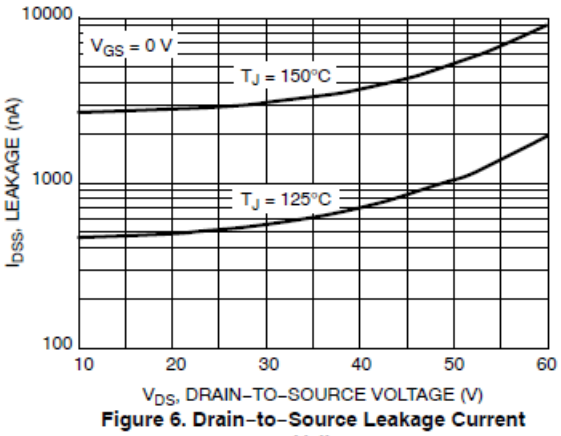

Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

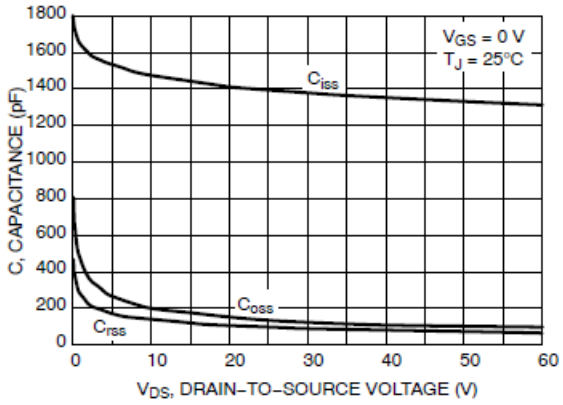

Figure 7. Capacitance Variation

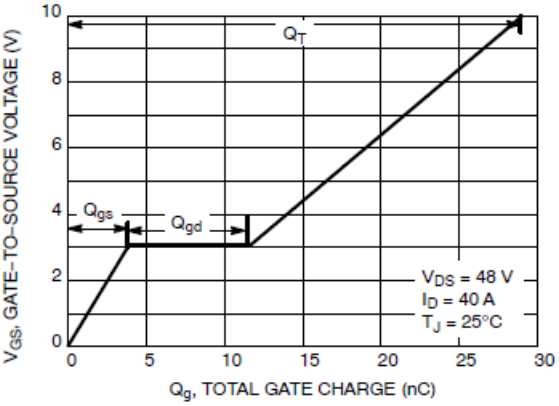

Figure 8. Gate–to–Source vs. Total Charge

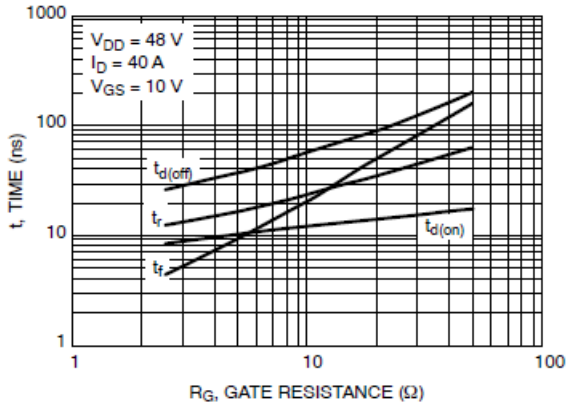

Figure 9. Resistive Switching Time Variation vs. Gate Resistance

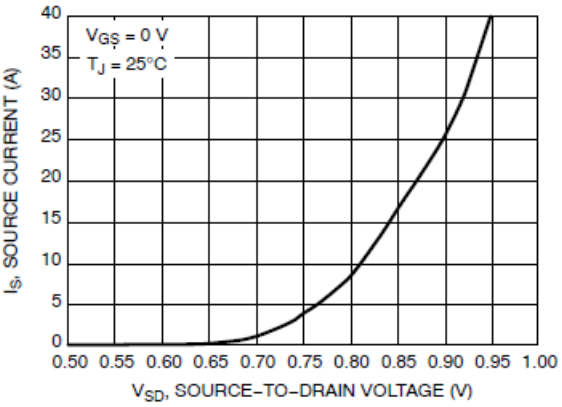

Figure 10. Diode Forward Voltage vs. Current

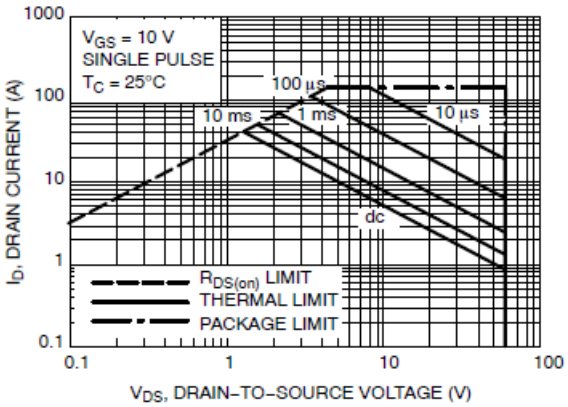

Figure 11. Maximum Rated Forward Biased Safe Operating Area

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