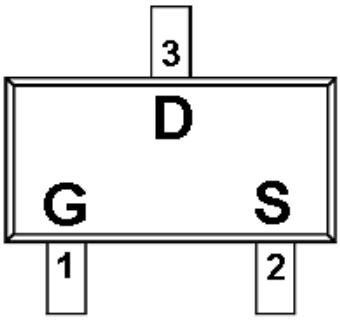
SPN3426
N-Channel Enhancement Mode MOSFET

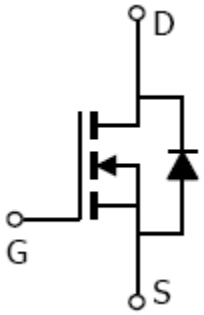
DESCRIPTION
The SPN3426 is the N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.
This high density process is especially tailored to minimize on-state resistance.
These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

APPLICATIONS
- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

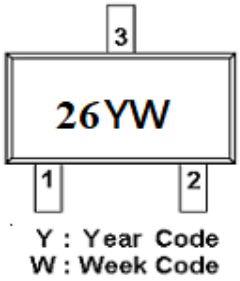
FEATURES
- 60V/3.0A,$R_{DS(ON)}$=90mΩ@V_{GS}=10V
- 60V/2.0A,$R_{DS(ON)}$=110mΩ@V_{GS}=4.5V
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23 package design

PIN CONFIGURATION (SOT–23)





PART MARKING



Y : Year Code
W : Week Code

SPN3426
N-Channel Enhancement Mode MOSFET

PIN DESCRIPTION

Pin	Symbol	Description
1	G	Gate
2	S	Source
3	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN3426S23RGB	SOT-23	26

※ Week Code : A ~ Z(1 ~ 26) ; a ~ z(27 ~ 52)
※ SPN3426S23RGB : Tape Reel ; Pb – Free ; Halogen – Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	60	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current(T_J=150℃)	T_A=25℃	I_D	3.0	A
	T_A=70℃		2.1	
Pulsed Drain Current		I_{DM}	16	A
Continuous Source Current(Diode Conduction)		I_S	1.5	A
Power Dissipation	T_A=25℃	P_D	1.6	W
	T_A=70℃		1.0	
Operating Junction Temperature		T_J	150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Ambient		$R_{\theta JA}$	75	℃/W

SPN3426
N-Channel Enhancement Mode MOSFET

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	60			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	1.0		2.5	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=48V,V_{GS}=0.0V			1	uA
		V_{DS}=48V,V_{GS}=0.0V T_J=55℃			5	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=3.0A		80	90	mΩ
		V_{GS}=4.5V,I_D=2.0A		100	110	
Forward Transconductance	gfs	V_{DS}=4.5V,I_D=3.0A		10		S
Diode Forward Voltage	V_{SD}	I_S=1.2A,V_{GS}=0V			1.1	V
Dynamic						
Total Gate Charge	Q_g	V_{DS}=15V,V_{GS}=10V I_D=6.7A		7		nC
Gate-Source Charge	Q_{gs}			1.2		
Gate-Drain Charge	Q_{gd}			3.0		
Input Capacitance	C_{iss}	V_{DS}=15V,V_{GS}=0V f=1MHz		410		pF
Output Capacitance	C_{oss}			50		
Reverse Transfer Capacitance	C_{rss}			26		
Turn-On Time	$t_{d(on)}$	V_{DD}=15V,R_L=15Ω I_D=1.0A,V_{GEN}=10V R_G=6Ω		6.0	11	nS
	t_r			8.0	18	
Turn-Off Time	$t_{d(off)}$			16	29	
	t_f			9	18	

TYPICAL CHARACTERISTICS

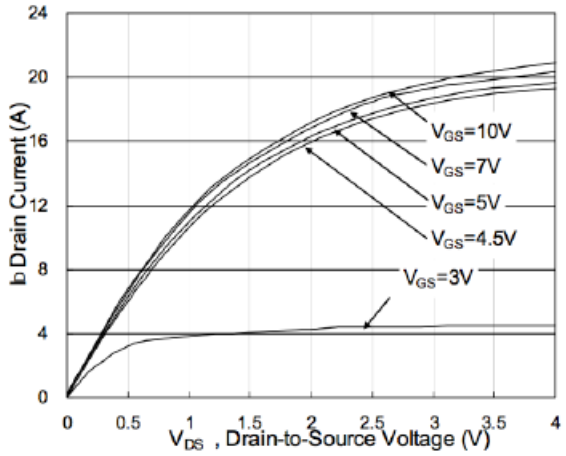


Fig.1 Typical Output Characteristics

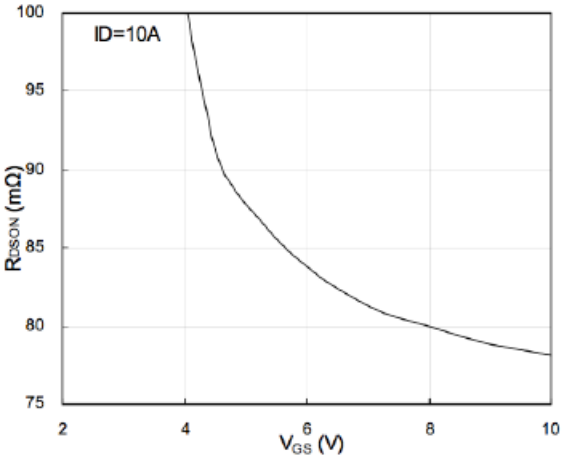


Fig.2 On-Resistance v.s Gate-Source

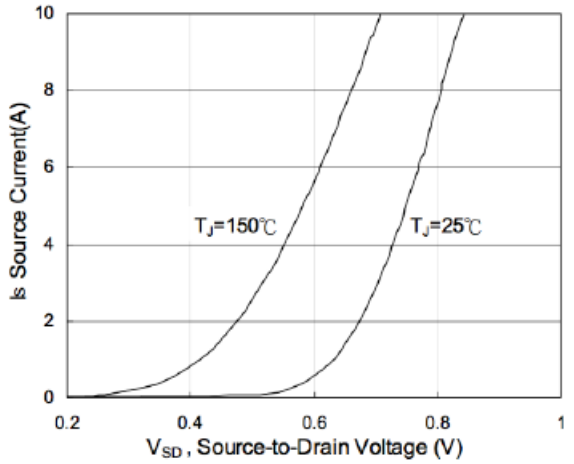


Fig.3 Forward Characteristics of Reverse

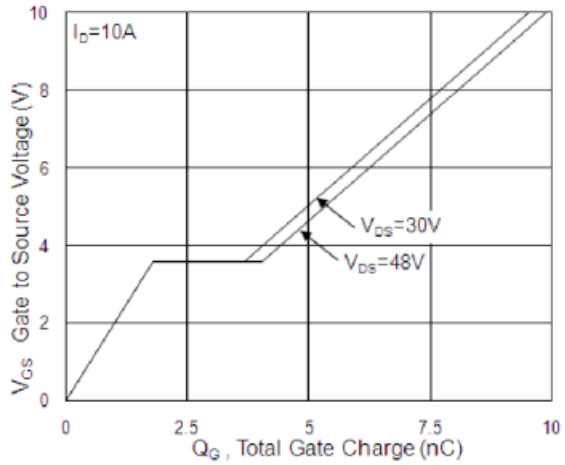


Fig.4 Gate-Charge Characteristics

TYPICAL CHARACTERISTICS

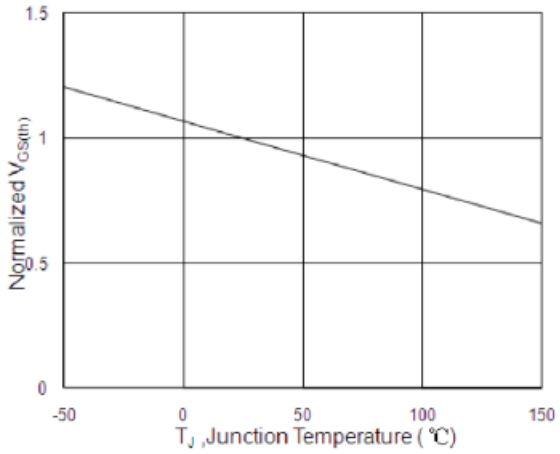


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

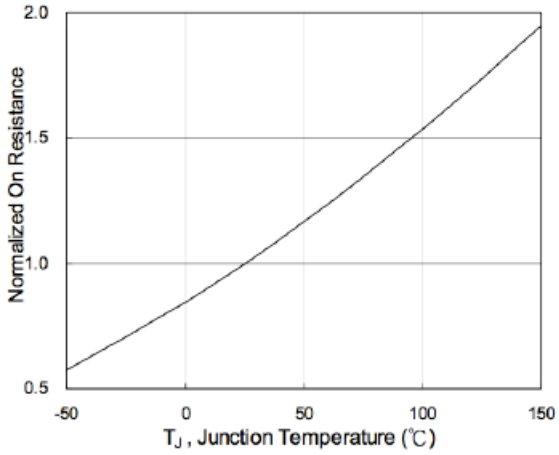


Fig.6 Normalized R_{DSON} v.s T_J

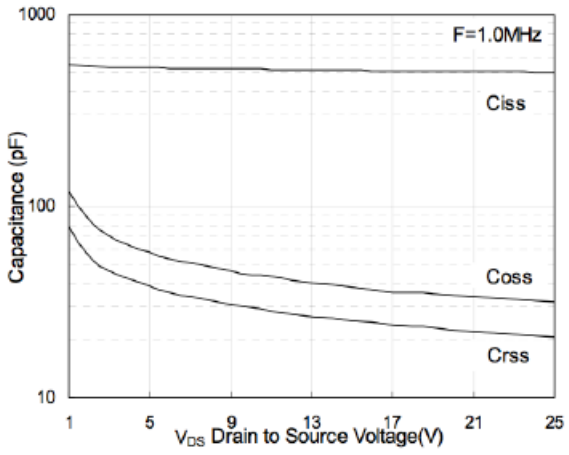


Fig.7 Capacitance

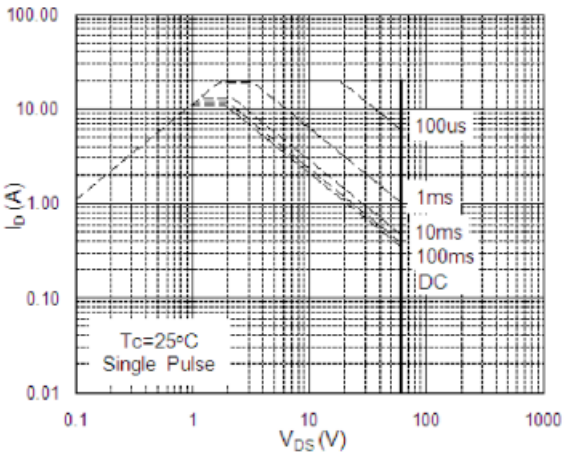


Fig.8 Safe Operating Area

SYNC Power Corporation
7F-2, No.3-1, Park Street
NanKang District (NKSP), Taipei, Taiwan, 115, R.O.C
Phone: 886-2-2655-8178
Fax: 886-2-2655-8468
© http://www.syncpower.com