



SPN340N06

N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN340N06 is the N-Channel enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed..

FEATURES

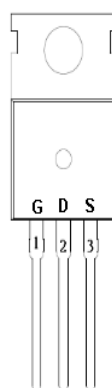
- ◆ 60V/340A, $R_{DS(ON)}=2.1m\Omega@V_{GS}=10V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ Enhanced Avalanche Ruggedness
- ◆ TO-220-3L/PPAK5x6 package design

APPLICATIONS

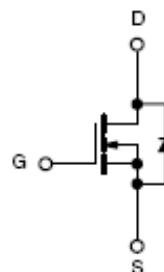
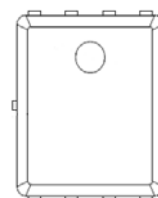
- DC/DC Converter
- Hard Switching and High Speed Circuit
- Synchronous Buck Converter
- Power Tools
- UPS
- Motor Control

PIN CONFIGURATION

TO-220-3L



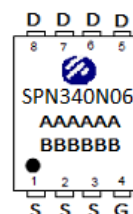
PPAK5x6



PART MARKING



A : Lot Code
B : Date Code



A : Lot Code
B : Date Code
(YY/MM/DD)



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PIN DESCRIPTION

PPAK5x6 PIN DESCRIPTION

Pin	Symbol	Description
1~3	S	Source
4	G	Gate
5~8	D	Drain

TO-220

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN340N06DN8RGB	PPAK5x6	SPN340N06
SPN340N06T220TGB	TO-220-3L	SPN340N06

※ SPN340N06DN8RGB: Tape&Reel; Pb – Free; Halogen – Free

※ SPN340N06 T220TGB: Tube ; Pb – Free; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	60	V
Gate –Source Voltage		V _{GSS}	±20	V
Continuous Drain Current(Silicon Limited)	Tc=25°C	I _D	363	A
	Tc=100°C		257	
Pulsed Drain Current		I _{DM}	900	A
Power Dissipation @ Tc=25°C	PPAK5x6	P _D	83	W
	TO-220		104	
Avalanche Energy with Single Pulse (Tc=25°C , L =0.1mH)		E _{AS}	180	mJ
Operating Junction Temperature		T _J	-55/150	°C
Storage Temperature Range		T _{STG}	-55/150	°C
Thermal Resistance-Junction to Case	PPAK5x6	R _{θJC}	1.5	°C/W
	TO-220		1.2	



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ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V,I _D =250uA	60			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} ,I _D =250uA	2	3	4	
Gate Leakage Current	I _{GSS}	V _{DS} =0V,V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V,V _{GS} =0V T _J = 25 °C			1	uA
		V _{DS} =60,V _{GS} =0V T _J =100 °C			100	
Drain-Source On-Resistance(PPAK5x6)	R _{DS(on)}	V _{GS} =10V,I _D =20A		1.9	2.1	mΩ
Drain-Source On-Resistance(TO220)				2.1	2.3	
Forward Transconductance	g _{fs}	V _{DS} =5V,I _D =20A		80		S
Gate Resistance	R _G	V _{GS} =0V,V _{DS} =Open, f=1MHz		0.63		Ω
Dynamic						
Total Gate Charge	Q _g	V _{DS} =30V,V _{GS} =10V I _D =20A		85		nC
Gate-Source Charge	Q _{gs}			24		
Gate-Drain Charge	Q _{gd}			14		
Input Capacitance	C _{iss}	V _{DS} =30V,V _{GS} =0V f=1MHz		7271		pF
Output Capacitance	C _{oss}			2042		
Reverse Transfer Capacitance	C _{rss}			61		
Turn-On Time	t _{d(on)}	V _{DD} =30V, I _D =20A, V _{GS} =10V, R _G =10Ω		35		nS
	t _r			62		
Turn-Off Time	t _{d(off)}			96		
	t _f			33		
Diode						
Diode Forward Voltage	V _{SD}	I _F =20A,V _{GS} =0V		0.9	1.2	V
Reverse Recovery Time	t _{rr}	V _R =30V, I _F =30A, dI _F /dt = 300A/uS		60		nS
Reverse Recovery Charge	Q _{rr}			175		nC



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TYPICAL CHARACTERISTICS



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Fig 1. Typical Output Characteristics

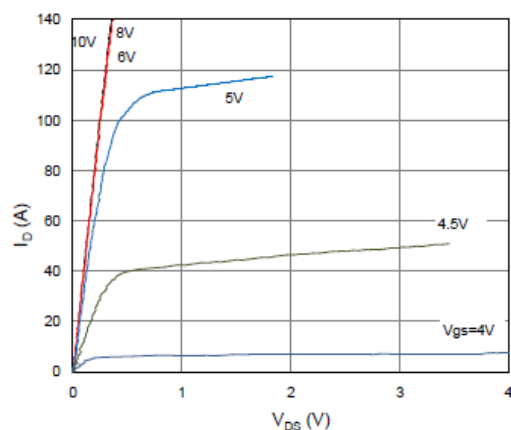


Figure 2. On-Resistance vs. Gate-Source Voltage

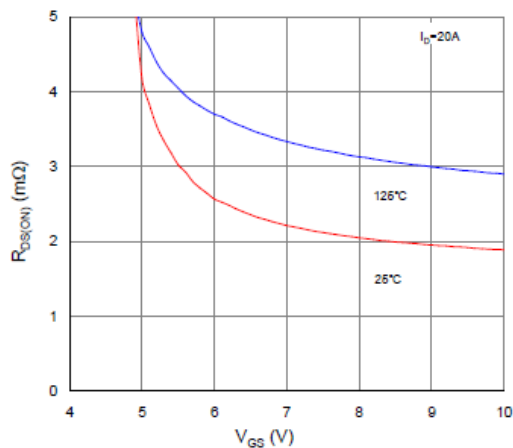


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

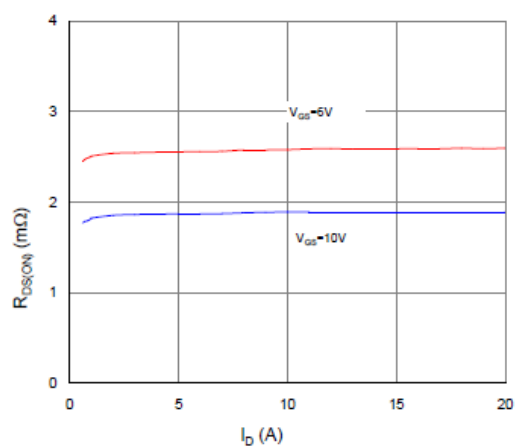


Figure 4. Normalized On-Resistance vs. Junction Temperature

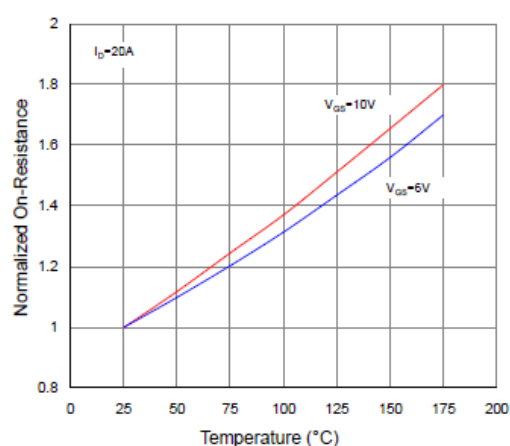


Figure 5. Typical Transfer Characteristics

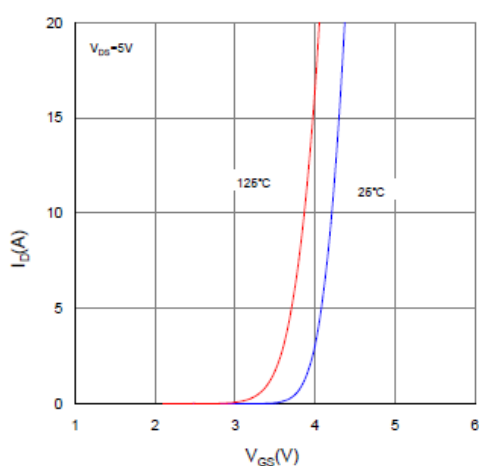
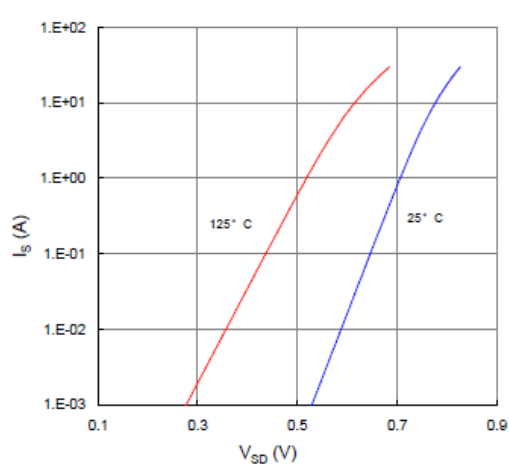


Figure 6. Typical Source-Drain Diode Forward Voltage



TYPICAL CHARACTERISTICS



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Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

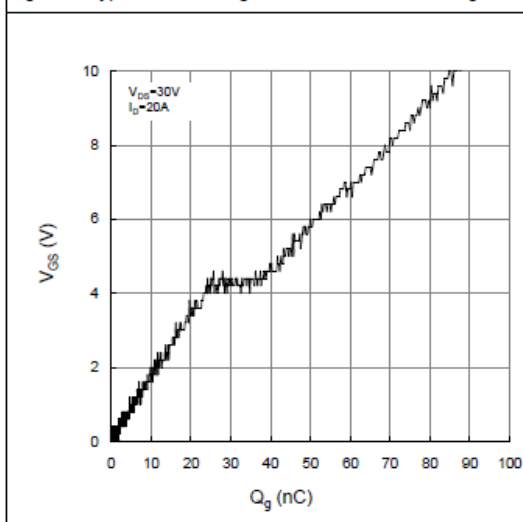


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

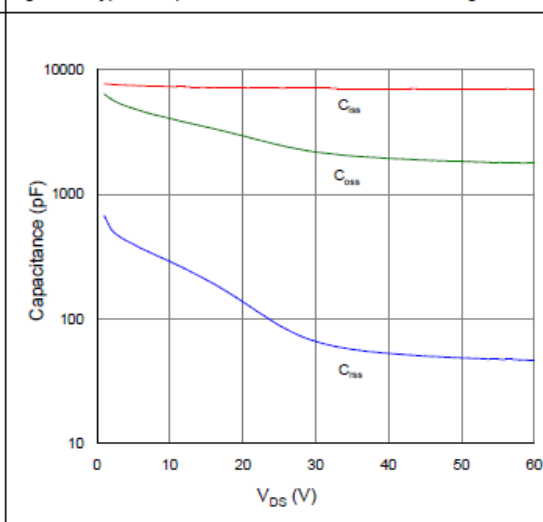


Figure 9. Maximum Safe Operating Area

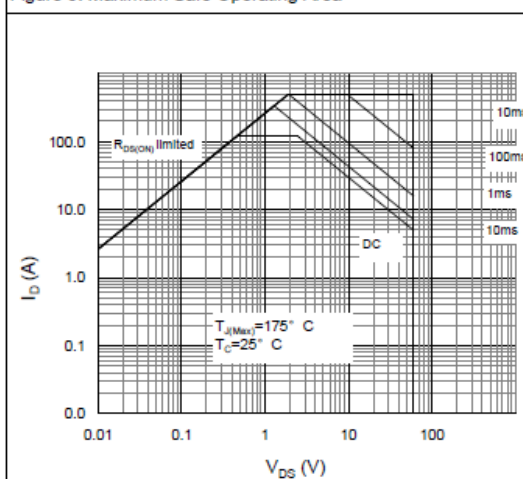


Figure 10. Maximum Drain Current vs. Case Temperature

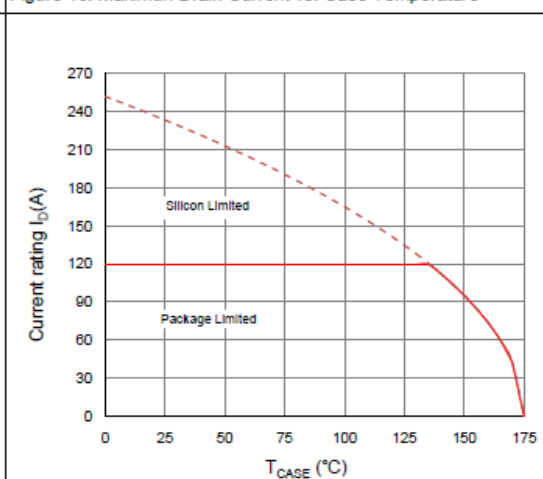
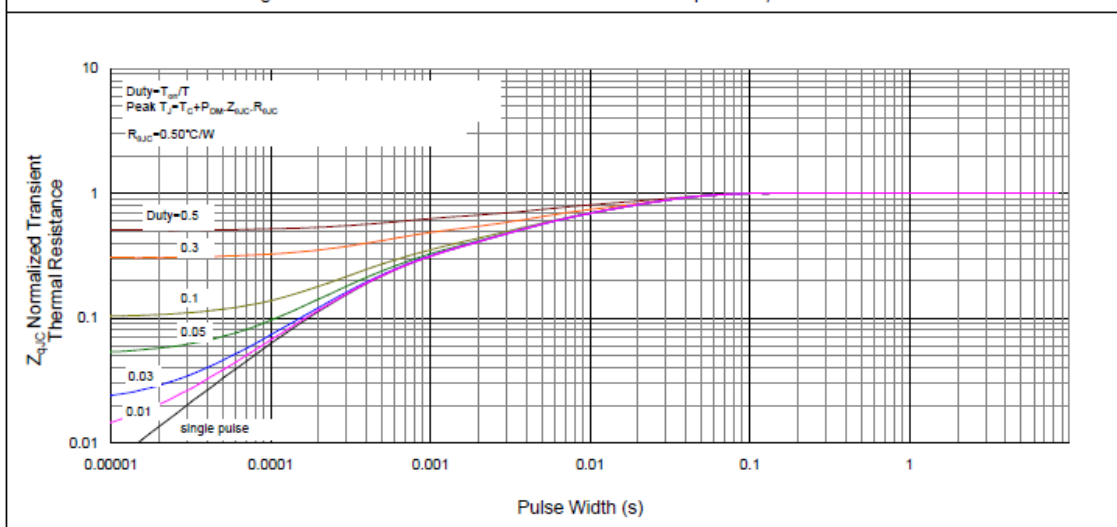


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case





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