



SPN2622

Dual N-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPN2622 is the Dual N-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where high-side switching , low in-line power loss, and resistance to transients are needed.

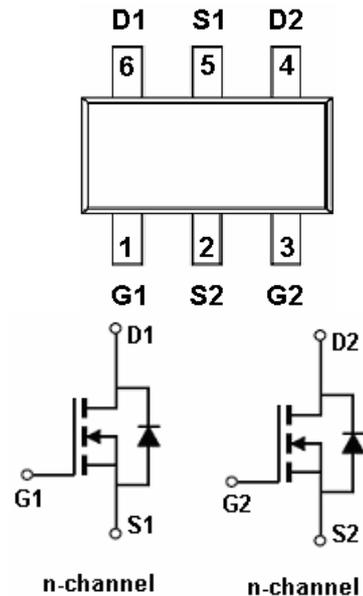
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

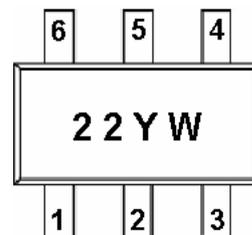
FEATURES

- 20V/4.0A, $R_{DS(ON)}=80m\Omega@V_{GS}=4.5V$
- 20V/3.4A, $R_{DS(ON)}=100m\Omega@V_{GS}=2.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23-6L package design

PIN CONFIGURATION(SOT-23-6L)



PART MARKING



Y : Year Code
W : Week Code



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PIN DESCRIPTION

Pin	Symbol	Description
1	G1	Gate 1
2	S2	Source 2
3	G2	Gate 2
4	D2	Drain 2
5	S1	Source 1
6	D1	Drain1

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN2622S26RGB	SOT-23-6L	22

※ Week Code : A ~ Z (1 ~ 26) ; a ~ z (27 ~ 52)

※ SPN2622S26RGB : Tape Reel ; Pb – Free; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

($T_A=25^{\circ}\text{C}$ Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V_{DSS}	20	V
Gate –Source Voltage	V_{GSS}	± 12	V
Continuous Drain Current($T_J=150^{\circ}\text{C}$)	I_D	$T_A=25^{\circ}\text{C}$	A
		$T_A=70^{\circ}\text{C}$	
Pulsed Drain Current	I_{DM}	10	A
Continuous Source Current(Diode Conduction)	I_S	1.6	A
Power Dissipation	P_D	$T_A=25^{\circ}\text{C}$	W
		$T_A=70^{\circ}\text{C}$	
Operating Junction Temperature	T_J	-55/150	$^{\circ}\text{C}$
Storage Temperature Range	T_{STG}	-55/150	$^{\circ}\text{C}$
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	105	$^{\circ}\text{C}/\text{W}$



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ELECTRICAL CHARACTERISTICS

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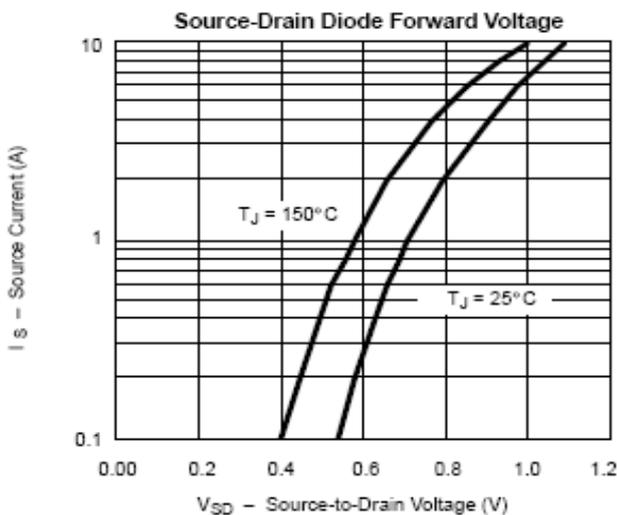
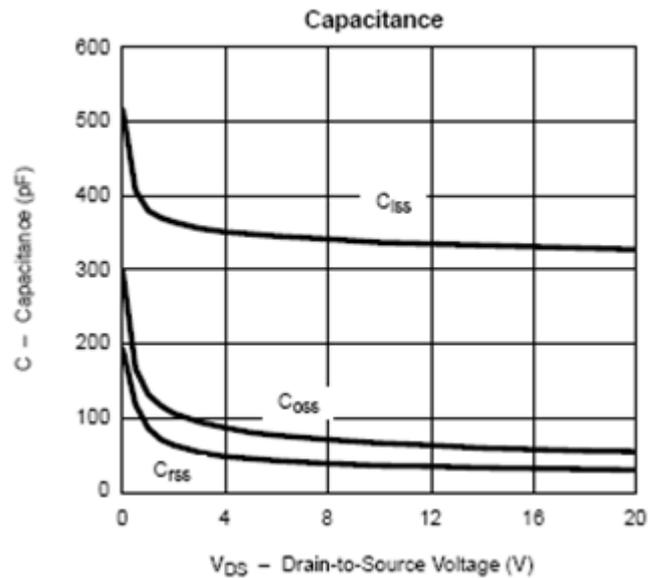
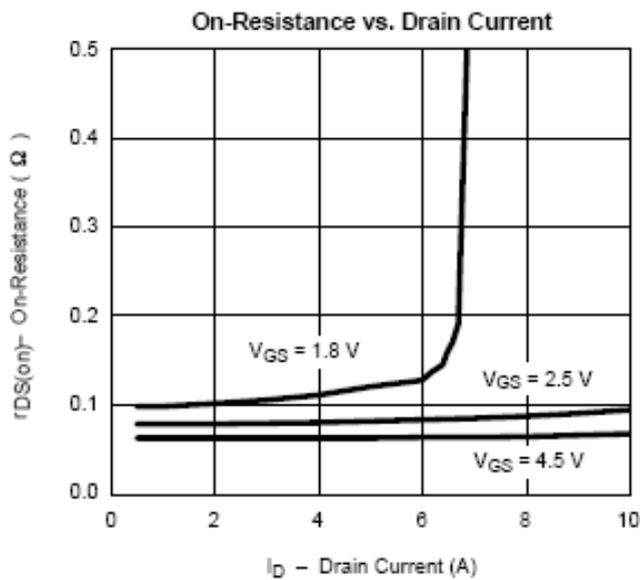
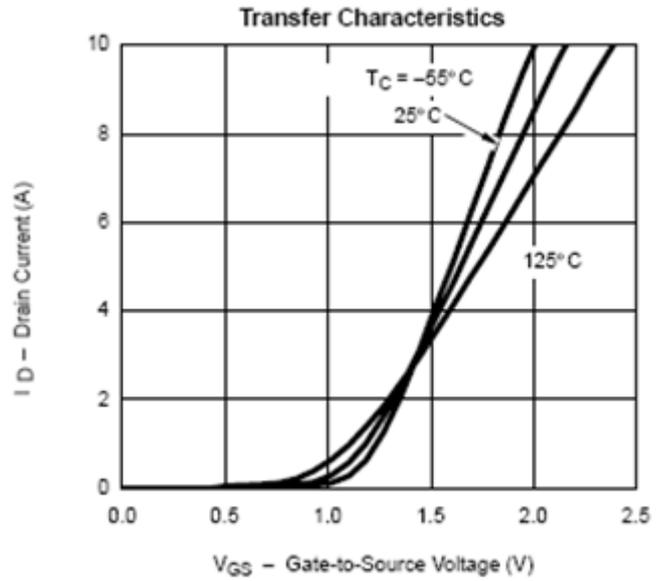
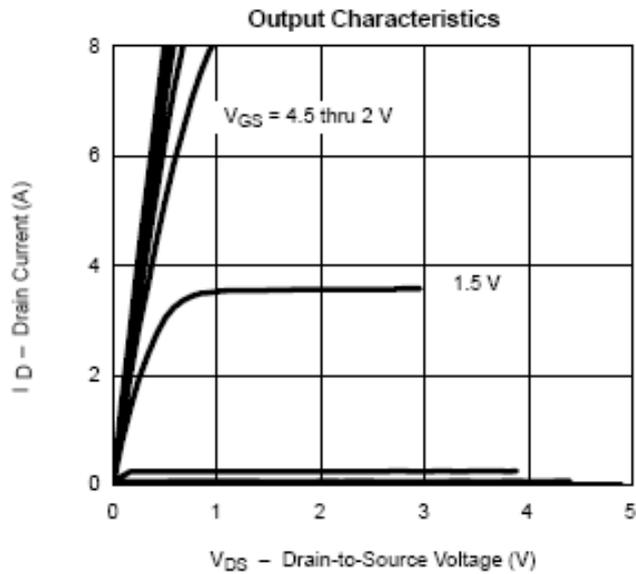
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.4		1.0	
Gate Leakage Current	I_{GSS}	$V_{DS}=0V, V_{GS}=\pm 12V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=20V, V_{GS}=0V$			1	uA
		$V_{DS}=20V, V_{GS}=0V$ $T_J=55^{\circ}\text{C}$			5	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \leq 5V, V_{GS}=4.5V$	6			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=4.0A$		0.060	0.080	Ω
		$V_{GS}=2.5V, I_D=3.4A$		0.075	0.100	
Forward Transconductance	g_{fs}	$V_{DS}=5V, I_D=-3.6A$		10		S
Diode Forward Voltage	V_{SD}	$I_S=1.6A, V_{GS}=0V$		0.8	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=6V, V_{GS}=4.5V$ $I_D=2.8A$		4.8	8	nC
Gate-Source Charge	Q_{gs}			1.0		
Gate-Drain Charge	Q_{gd}			1.0		
Input Capacitance	C_{iss}	$V_{DS}=6V, V_{GS}=0V$ $f=1\text{MHz}$		485		pF
Output Capacitance	C_{oss}			85		
Reverse Transfer Capacitance	C_{rss}			40		
Turn-On Time	$t_{d(on)}$	$V_{DD}=6V, R_L=6\Omega$ $I_D=1.0A, V_{GEN}=4.5V$ $R_G=6\Omega$		8	14	nS
	t_r			12	18	
Turn-Off Time	$t_{d(off)}$			30	35	
	t_f			12	16	



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TYPICAL CHARACTERISTICS

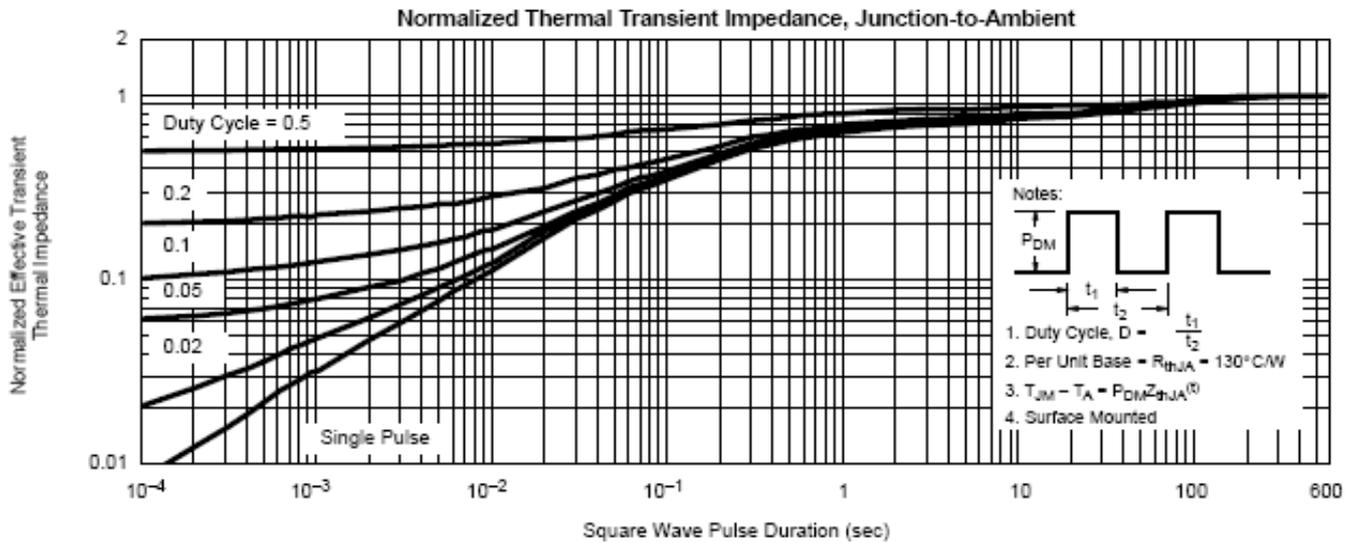
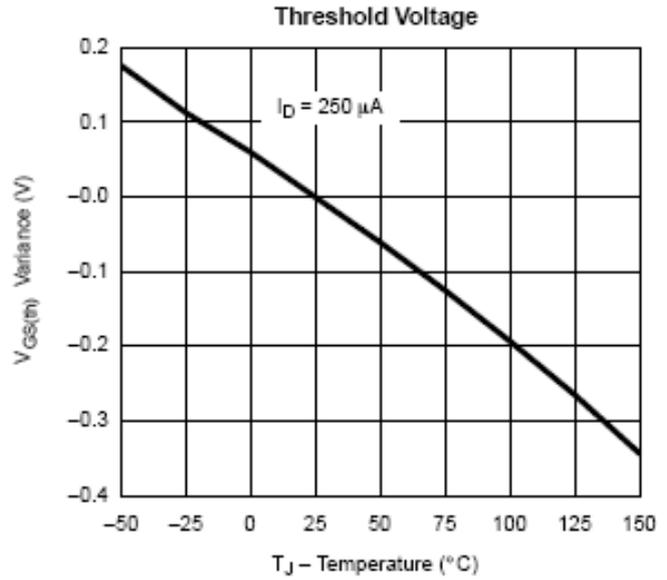
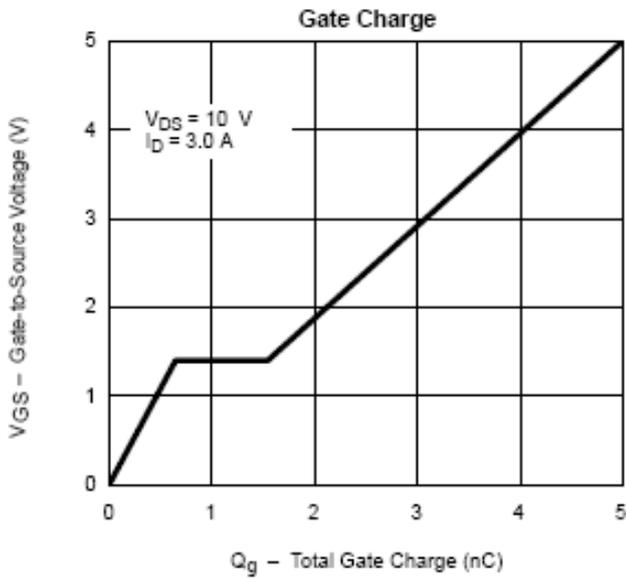




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TYPICAL CHARACTERISTICS





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SYNC Power Corporation

7F-2, No.3-1, Park Street

NanKang District (NKSP), Taipei, Taiwan 115

Phone: 886-2-2655-8178

Fax: 886-2-2655-8468

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