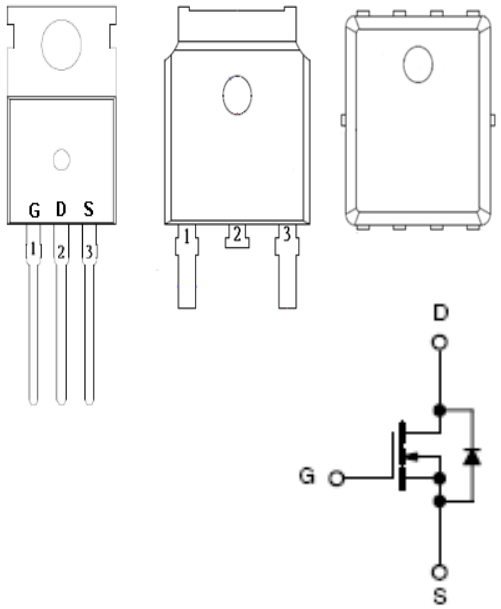
SPN166T04A
N-Channel Enhancement Mode MOSFET

DESCRIPTION
The SPN166T04A is the N-Channel enhancement mode power field effect transistor which is produced using super high cell density DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suitable for synchronous rectifier application, Motor control power management and other Power Tool circuits. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

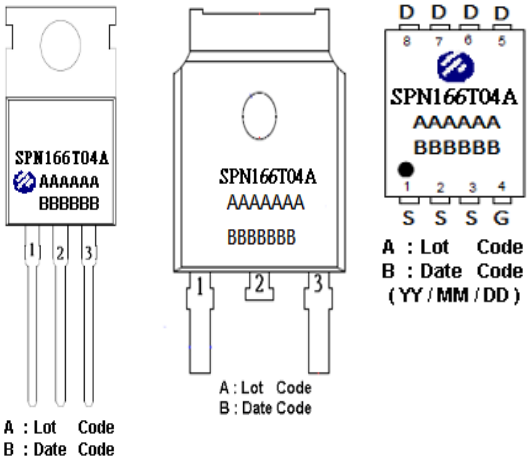
APPLICATIONS
- DC/DC Converter
- Load Switch
- SMPS Secondary Side Synchronous Rectifier
- Motor Control
- Power Tool

FEATURES
- 45V/166A, $R_{DS(ON)}$=3.2mΩ@V_{GS}=10V
- Super high density cell design for extremely low $R_{DS\ (ON)}$
- Exceptional on-resistance and maximum DC current capability
- TO-220-3L/ TO-252-2L/PPAK5x5-8L package design

PIN CONFIGURATION
TO-220-3L TO-252-2L PPAK5x6-8L



PART MARKING



PIN DESCRIPTION (TO-220-3L/TO-252-2L)

Pin	Symbol	Description
1	G	Gate
2	D	Drain
3	S	Source

PIN DESCRIPTION (PPAK5x6-8L)

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPN166T04AT220TGB	TO-220-3L	SPN166T04A
SPN166T04AT252RGB	TO-252-2L	SPN166T04A
SPN166T04ADN8RGB	PPAK5x6-8L	SPN166T04A

※ SPN166T04AT220TGB : Tube ; Pb – Free ; Halogen – Free

※ SPN166T04AT252RGB : Tape& Reel ; Pb – Free ; Halogen – Free

※ SPN166T04ADN8RGB : Tape& Reel ; Pb – Free ; Halogen – Free

SPN166T04A
N-Channel Enhancement Mode MOSFET

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V_{DSS}	45	V
Gate –Source Voltage		V_{GSS}	±20	V
Continuous Drain Current (Silicon Limited) (TO-220/TO-252)	Tc=25℃	I_D	166	A
	Tc=100℃		118	
Continuous Drain Current (Silicon Limited) (PPAK5x6)	Tc=25℃	I_D	140	A
	Tc=100℃		89	
Pulsed Drain Current		I_{DM}	350	A
Power Dissipation @ Tc=25℃	TO-220	P_D	104	W
Power Dissipation @ Tc=25℃	TO-252		93	
Avalanche Energy with Single Pulse (T_C=25℃, L=0.5mH.)		E_{AS}	100	mJ
Operating Junction Temperature		T_J	-55/150	℃
Storage Temperature Range		T_{STG}	-55/150	℃
Thermal Resistance-Junction to Case (TO-220)		$R_{\theta JC}$	1.2	℃/W
Thermal Resistance-Junction to Case (TO-252)		$R_{\theta JC}$	1.35	℃/W
Thermal Resistance-Junction to Case (PPAK5x6)		$R_{\theta JC}$	1.5	℃/W

Note :

The maximum current rating is package limited at 120A for TO-220-3L
The maximum current rating is package limited at 70A for TO-252-2L
The maximum current rating is package limited at 80A for PPAK5x6-8L

ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250uA	45			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	2.0	2.5	4.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=36V,V_{GS}=0V T_J = 25 ℃			1	uA
		V_{DS}=36V, V_{GS}=0V T_J = 100 ℃			100	
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=20A		2.5	3.2	mΩ
Forward Transconductance	gfs	V_{DS}=5V,I_D=20A		85		S
Gate Resistance	R_G	V_{GS}=0V,V_{DS} open, f=1MHz		1.5		Ω
Diode Forward Voltage	V_{SD}	I_S=20A,V_{GS}=0V		0.9	1.2	V
Dynamic						
Total Gate Charge (10V)	Q_g	V_{DS}=20V,V_{GS}=10V I_D=20A		54		nC
Gate-Source Charge	Q_{gs}			14		
Gate-Drain Charge	Q_{gd}			7		
Input Capacitance	C_{iss}	V_{DS}=20V,V_{GS}=0V f=1MHz		3834		pF
Output Capacitance	C_{oss}			1348		
Reverse Transfer Capacitance	C_{rss}			70		
Turn-On Time	td(on)	V_{DD}=20V, ID=20A V_{GEN}=10V, R_G=10Ω		14		nS
	tr			12		
Turn-Off Time	td(off)			58		
	tf			15		

TYPICAL CHARACTERISTICS

Fig 1. Typical Output Characteristics

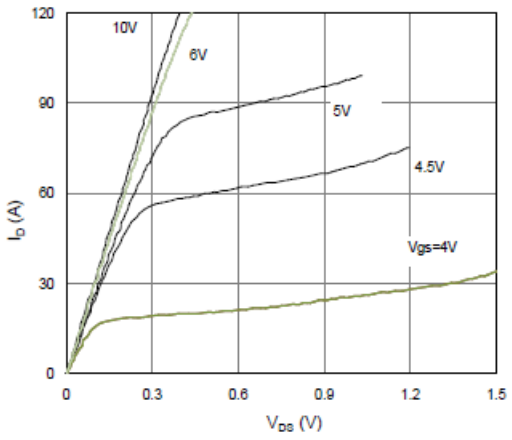


Figure 2. On-Resistance vs. Gate-Source Voltage

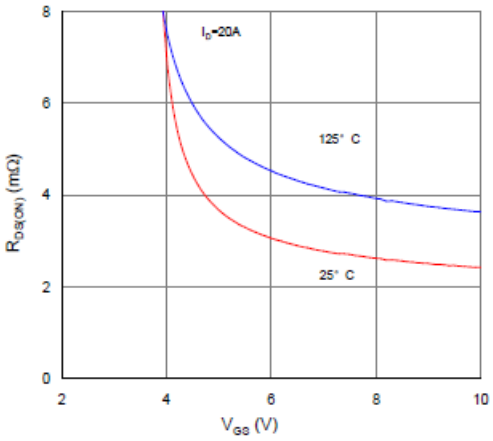


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

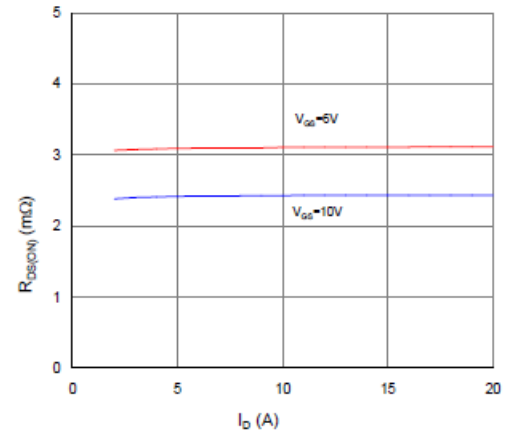


Figure 4. Normalized On-Resistance vs. Junction Temperature

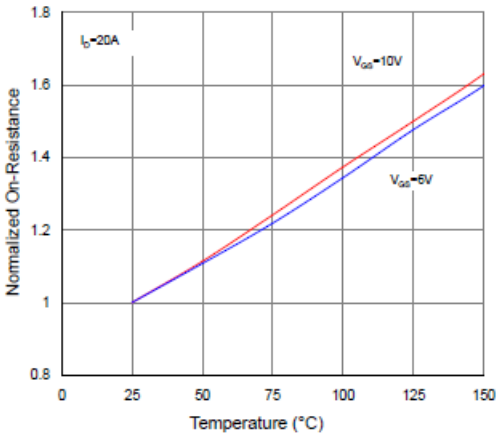


Figure 5. Typical Transfer Characteristics

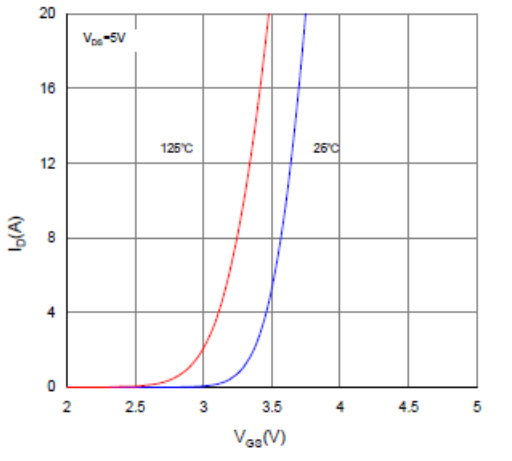
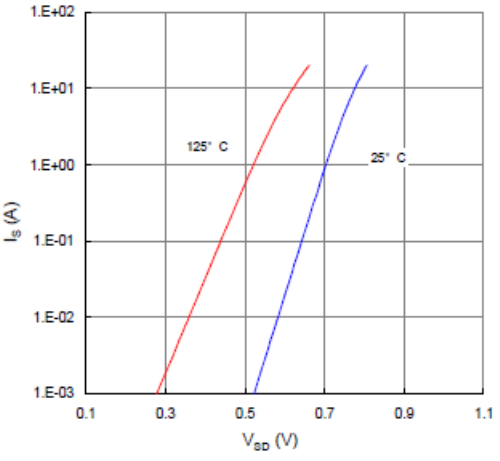


Figure 6. Typical Source-Drain Diode Forward Voltage



TYPICAL CHARACTERISTICS

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

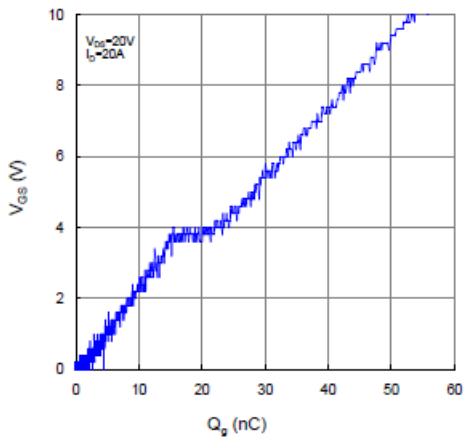


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

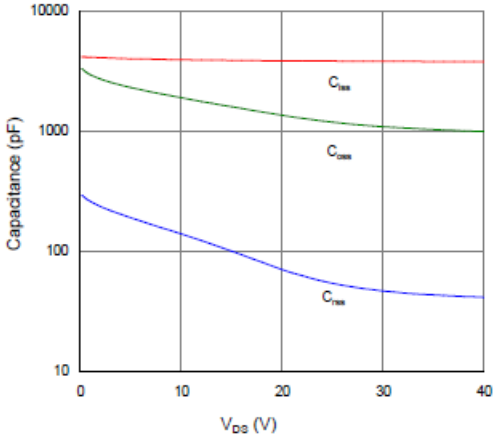


Figure 9. Maximum Safe Operating Area

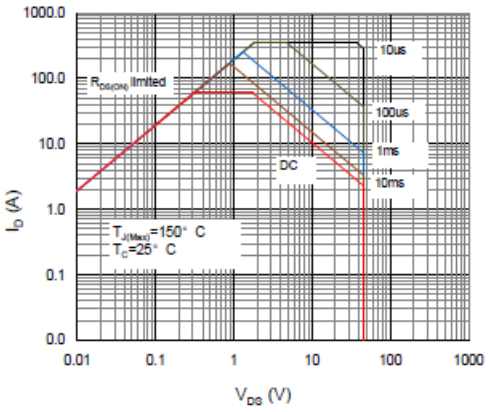


Figure 10. Maximun Drain Current vs. Case Temperature

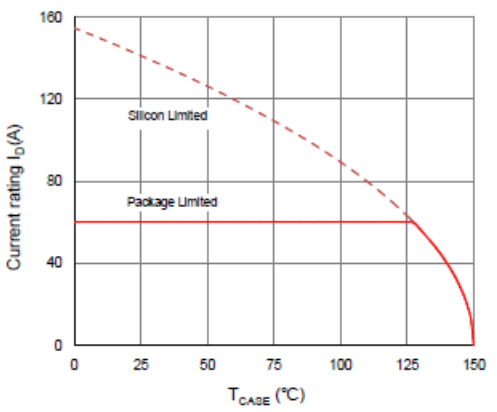
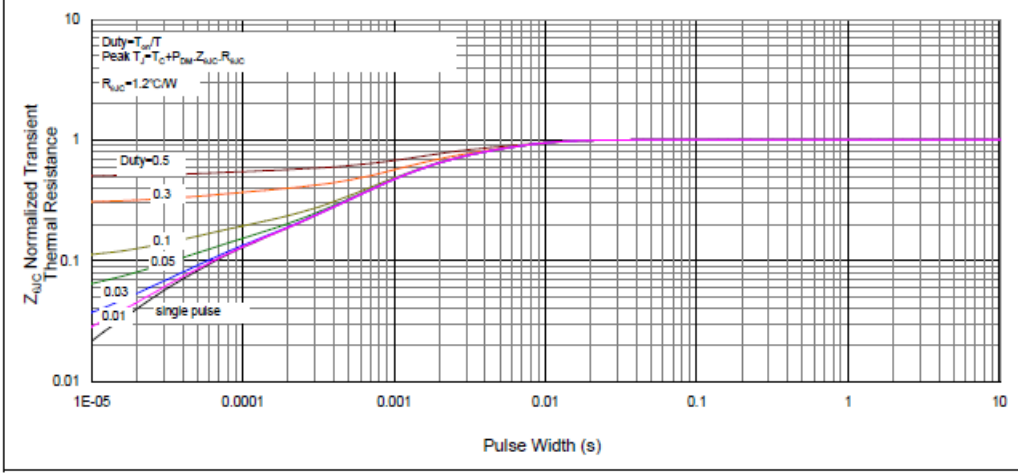


Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



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